UCC27714 High-Speed, 600-V High-Side Low-Side Gate Driver with 4-A Peak Output

1 Features

- High-Side, Low-Side Configuration, with Independent Inputs
- Fully Operational up to 600 V (HS Pin)
- Floating Channel Designed for Bootstrap Operation
- Peak Output Current Capability of 4-A Sink 4-A Source at VDD = 15 V
- Best-In-Class Propagation Delay (125-ns Maximum)
- Best-In-Class Delay Matching (20-ns Maximum)
- TTL and CMOS Compatible Input Logic
- VDD Bias Supply Range of 10 V to 20 V
- Bias UVLO Protection for Both Channels
- Rail-to-Rail Drive
- Robust Operation Under Negative Voltage Transients
- High dv/dt Immunity (HS Pin)
- Separated Grounds for Logic (VSS) and Driver (COM) with Capability to Sustain Voltage Difference
- Optional Enable Function (Pin 4)
- Outputs Held in LOW when Inputs Floating
- Inputs and Enable Pin Voltage Levels Not Restricted by VDD Pin Bias Supply Voltage
- High and Low Voltage Pins Separated for Maximum Creepage and Clearance
- Negative Voltage Handling Capability on Input and Enable Pins

2 Applications

- Half-Bridge and Full-Bridge Converters in Offline AC and DC Power Supplies
- High-Density Switching Power Supplies for Server, Telecom, IT and Industrial Infrastructure
- Solar Inverters, Motor Drive and UPS

3 Description

UCC27714 is a 600-V high-side, low-side gate driver with 4-A source and 4-A sink current capability, targeted to drive power MOSFETs or IGBTs. The device comprises of one ground-referenced channel (LO) and one floating channel (HO) which is designed for operating with bootstrap supplies. The device features excellent robustness and noise immunity with capability to maintain operational logic at negative voltages of up to –8 V_{DC} on HS pin (at VDD = 12 V).

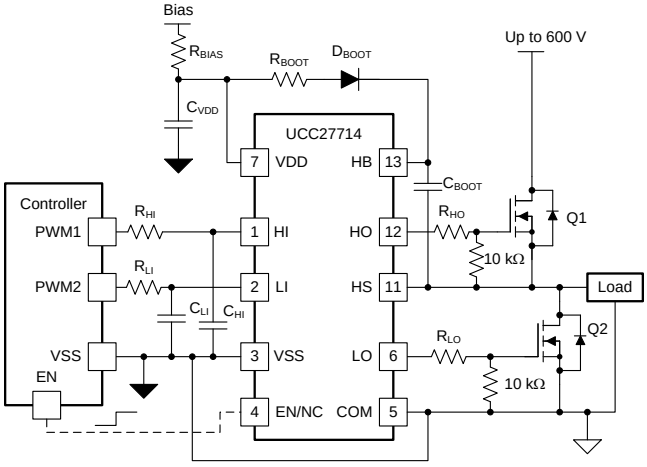
The device accepts a wide range bias supply input from 10 V to 20 V and offers UVLO protection for both the VCC and HB bias supply pins. UCC27714 is available in SOIC-14 package and rated to operate from –40°C to 125°C.

Device Information(1)

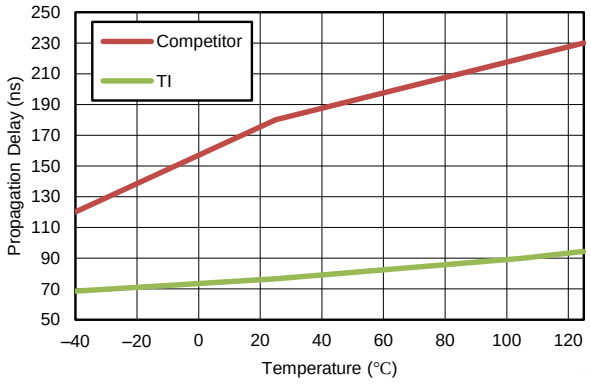
PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC27714	SOIC (14)	3.91 mm × 8.65 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



Typical Propagation Delay Comparison



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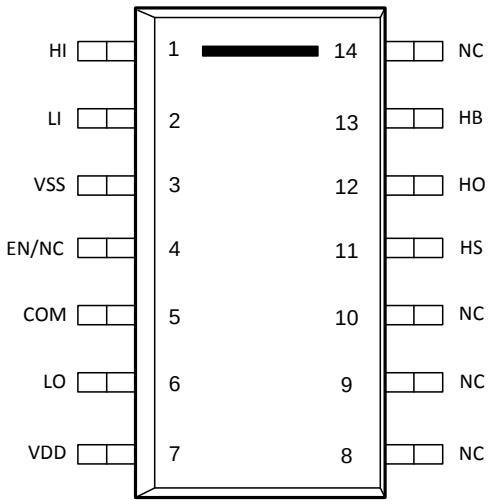
5 Revision History

Changes from Original (August, 2015) to Revision A	Page
• Changed marketing status from Product preview to Final.	1

6 Pin Configuration and Functions

D Package
14-Pin SOIC
Top View



Terminal Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COM	5	–	Return for low-side driver output.
EN/NC	4	I	Enable input for high-side and low-side driver. This pin biased LOW, disables both HO and LO regardless of HI and LI state, This pin biased high or floating enables both HO and LO.
HB	13	I	High-side floating supply. Bypass this pin to HS with a suitable capacitor to sustain boot-strap circuit operation in the desired application, typically 10× bigger than gate capacitance.
HI	1	I	Logic input for high-side driver. If HI is unbiased or floating, HO is held low.
HO	12	O	High-side driver output.
HS	11	–	Return for high-side floating supply.
LI	2	I	Logic input for low-side driver. If LI is unbiased or floating, LO is held low.
LO	6	O	Low-side driver output.
NC	8, 9, 10, 14	–	No connection.
VDD	7	I	Bias supply input. Power supply for the input logic side of the device and also low-side driver output. Bypass this pin to VSS with typical 1-µF SMD capacitor (typically C_{VDD} needs to be 10 × C_{BOOT}). If shunt resistor used between COM and VSS, then also bypass this pin to COM with 1-µF SMD capacitor.
VSS	3	–	Logic ground.

7 Specifications

7.1 Absolute Maximum Ratings (1) (2)

Over operating free-air temperature range (unless otherwise noted), all voltages are with respect to COM (unless otherwise noted), currents are positive into and negative out of the specified terminal. (1)

			MIN	MAX	UNIT
V_{IN}	Input voltage range	HI, LI, EN(3) with respect to VSS	–5	20	V
		VDD supply voltage	–0.3	20	V
		HB	–0.3	640	V
		HB-HS	–0.3	20	V
V_{OUT}	Output voltage range, HO	DC	HS – 0.3	HB + 0.3	V
		Transient, less than 100 ns(4)	HS – 2	HB + 0.3	V
	Output voltage range, LO	DC	–0.3	VDD + 0.3	V
		Transient, less than 100 ns(4)	–2	VDD + 0.3	V
	Logic ground, With respect to COM		–7	6	V
	Logic ground, VDD-VSS		–0.3	20	V
I_{OUT}	Output current, HO, LO, IOUT_PULSED (100 ns)			±4	A
I_{OUT}	Output current, HO, LO, IOUT_DC			0.25	A
dV_{HS}/dt	Allowable offset supply voltage transient		–50	50	V/ns
	Lead temperature (soldering, 10 second)			300	°C
T_J	Junction temperature range		–40	150	°C
T_{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See Packaging Section of the datasheet for thermal limitations and considerations of packages.
(3) The maximum voltage on the Input pins is not restricted by the voltage on the VDD pin.
(4) Values are verified by characterization on bench.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$[1] Electrostatic discharge	Human body model, HBM	±1400	V
	Charge device model, CDM	±500	V

(1) These devices are sensitive to electrostatic discharge; follow proper device handing procedures

7.3 Recommended Operating Conditions

All voltages are with respect to COM, –40°C < T_J < 125°C, currents are positive into, negative out of the specified terminals

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	10		18	V
HB-HS	Driver bootstrap voltage	10		18	V
HS	Source terminal voltage[1]	–8		600	V
HB	Bootstrap pin voltage	HS + 10		HS + 18	V
HI, LI, EN	Input voltage with respect to VSS	–4		18	V
VSS	Logic ground	–6[2]		5[3]	V
T_J	Junction temperature	–40		125	°C

(1) Logic operational for HS of –8 V to 600 V at HB – HS = 12 V
(2) At VDD – COM = 10 V
(3) At VDD – COM = 15 V

7.4 Thermal Information

THERMAL METRIC[1]		UCC27714 D (SOIC) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

At VDD = VHB = 15 V, VSS = VHS = 0, all voltages are with respect to COM, no load on LO and HO, –40°C < T_J < 125°C, current are positive into and negative out of the specified terminal, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY BLOCK						
$V_{VDD(on)}$	turn-on threshold voltage of VDD		8.4	9.1	9.8	V
$V_{VDD(off)}$	turn-off threshold voltage of VDD		7.9	8.6	9.3	V
$V_{VDD(hys)}$	Hysteresis of VDD		0.4	0.5	-	V
$V_{VHB(on)}$	turn-on threshold voltage of VHB-VHS		7.7	8.3	9.0	V
$V_{VHB(off)}$	turn-off threshold voltage of VHB-VHS		6.7	7.25	8.05	V
$V_{VHB(hys)}$	Hysteresis of VHB-VHS		0.5	1.0	-	V
I_{QDD}	Total quiescent VDD to VSS and COM supply current	HI = LI = 0 V or 5 V, DC on/off state		750	1050	µA
I_{QCOM}	Quiescent VDD-COM supply current	HI = LI = 0 V or 5 V, DC on/off state		175	350	µA
I_{QVSS}	Quiescent VDD-VSS supply current	HI = LI = 0 V or 5 V, DC on/off state		550	750	µA
I_{QBS}	Quiescent HB-HS supply current	HI = 0 V or 5 V, HO in DC on/off state		120	300	µA
I_{BL}	Bootstrap Supply Leakage Current	HB = HS = 600 V			20	µA
INPUT AND ENABLE BLOCK						
V_{INH}, V_{ENH}	Input pin (HI or LI) and enable pin (EN) High threshold		1.7	2.3	2.7	V
V_{INL}, V_{ENL}	Input pin (HI or LI) and enable pin (EN) low threshold		1.2	1.6	2.1	V
V_{INHYS}, V_{ENHYS}	Input pin (HI or LI) and enable pin (EN) threshold hysteresis			0.7		V
I_{INL}	HI, LI input low bias current	HI, LI = 0 V	-5	0	5	µA
I_{INH}	HI, LI input high bias current	HI, LI = 5 V	3		65	µA
I_{ENL}	EN input low bias current	V_{EN} = 0 V	-90		-50	µA
I_{ENH}	EN input high bias current	V_{EN} = 5 V	-65		-25	µA
R_{HI}	Pull-down resistor on HI input pin			400		kΩ
R_{LI}	Pull-down resistor on LI input pin			400		kΩ
R_{EN}	Pull-up resistor on enable pin			200		kΩ
OUTPUT BLOCK						
V_{DD}-V_{LOH}	LO output high voltage	LI = 5 V, I_{LO} = –20 mA		70	120	mV
V_{HB}-V_{HOH}	HO output high voltage	HI = 5 V, I_{HO} = –20 mA		70	120	mV
V_{LOL}	LO output low voltage	LI = 0 V, I_{LO} = 20 mA		15	35	mV
V_{HOL}	HO output low voltage	HI = 0 V, I_{HO} = 20 mA		20	40	mV
R_{LOL}, R_{HOL} (1)	LO, HO output pull down resistance	I_{LO} = 20 mA, I_{HO} = 20 mA			1.45	Ω
R_{LOH}, R_{HOH}	LO, HO output pull up resistance	I_{LO} = –20 mA, I_{HO}= –20 mA		3.75	5.8	Ω
I_{GPK-} (2)	HO. LO output low short circuit pulsed current	HI = L = 0 V, HO = LO = 15 V, PW < 10 µs		4		A
I_{GPK+} (2)	HO. LO output high short circuit pulsed current	H I= LI = 5 V, HO = LO = 0 V, PW < 10 µs		4		A

(1) R_{OH} represents on-resistance of only the P-Channel MOSFET device in pull-up structure of UCC27714 output stage. Refer to Output Stage

(2) Ensured by Design, Not tested in production

7.6 Timing Requirements

		MIN	NOM	MAX	UNIT
DYNAMIC CHARACTERISTICS					
t_{PDLH}	Turn-on propagation delay, LI to LO, HI to HO, HS = COM = 0 V or HS = 600 V		90	125	ns
t_{PDHL}	Turn-off propagation delay, LI to LO, HI to HO, HS = COM = 0 V or HS = 600 V		90	125	ns
t_{PDRM}	Low-to-high delay matching, HS = COM = 0 V			20	ns
t_{PDFM}	High-to-low delay matching, HS = COM = 0 V			20	ns
t_{RISE}	Turn-on rise time, 10% to 90%, HO/LO with 1000-pF load		15	30	ns
t_{FALL}	Turn-off fall time, 90% to 10%, HO/LO with 1000-pF load		15	30	ns
t_{ON}	Minimum HI/LI ON pulse that changes output state, 0-V to 5-V input signal on HI and LI pins			100	ns
t_{OFF}	Minimum HI/LI OFF pulse that changes output state, 5-V to 0-V input signal on HI and LI pins			100	ns

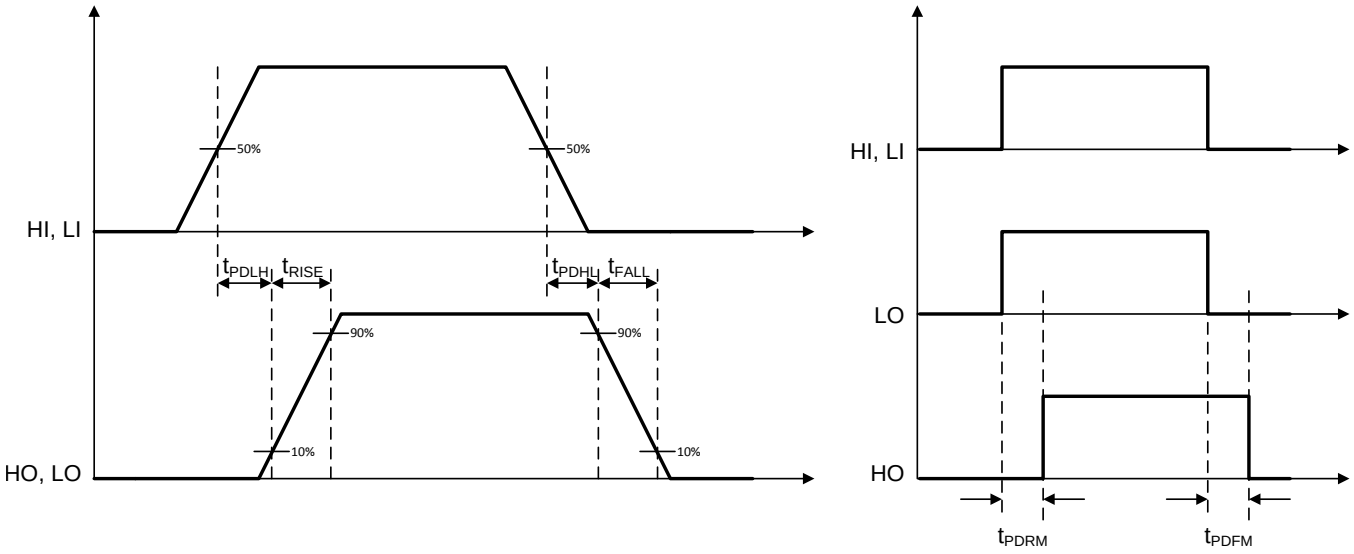


Figure 1. Typical Test Timing Diagram

7.7 Typical Characteristics

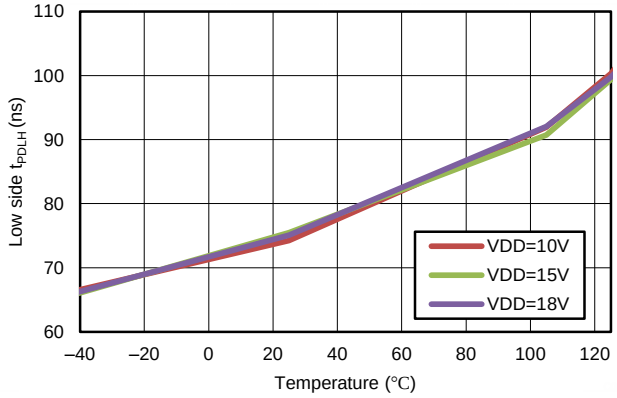


Figure 2. Low-Side, Turn-On Propagation Delay vs Temperature

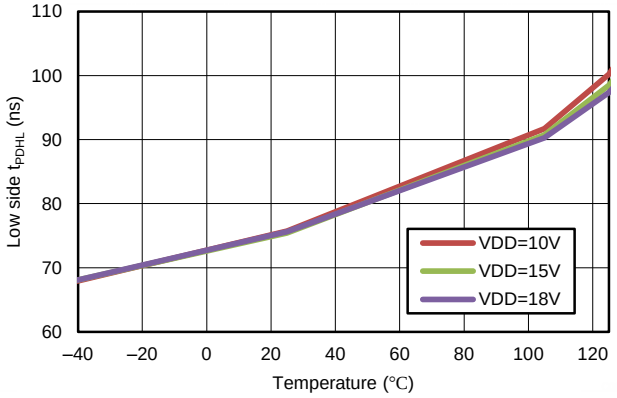


Figure 3. Low-Side, Turn-Off Propagation Delay vs Temperature

Typical Characteristics (continued)

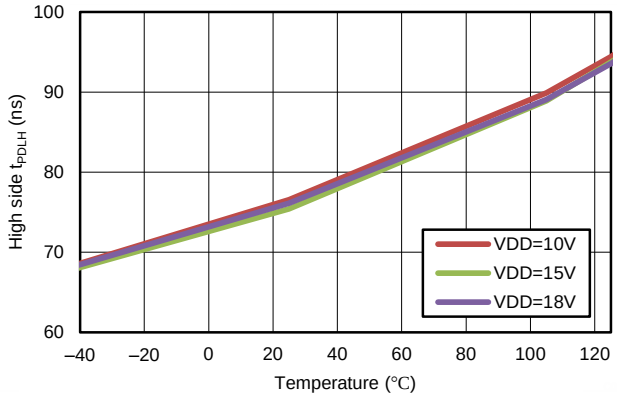


Figure 4. High-Side, Turn-On Propagation Delay vs Temperature

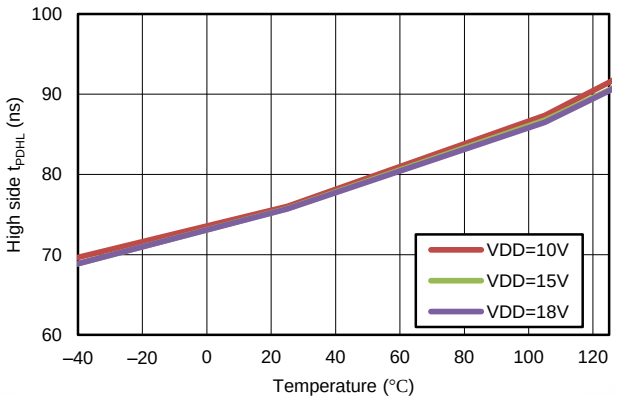


Figure 5. High-Side, Turn-Off Propagation Delay vs Temperature

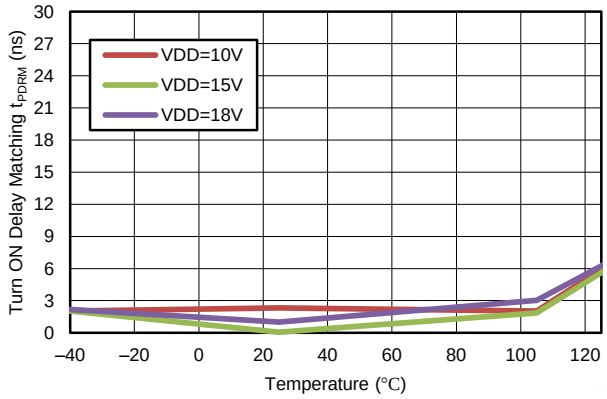


Figure 6. Turn-On Delay Matching vs Temperature

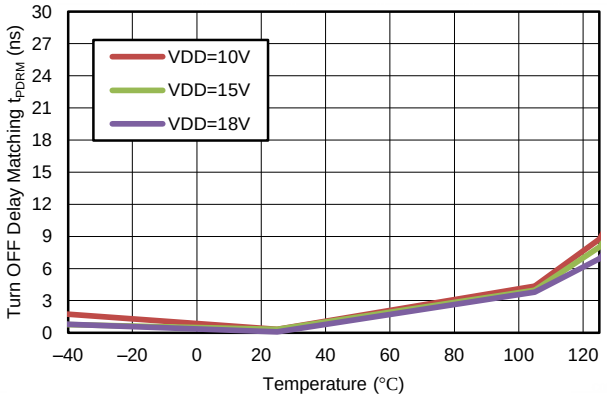


Figure 7. Turn-Off Delay Matching vs Temperature

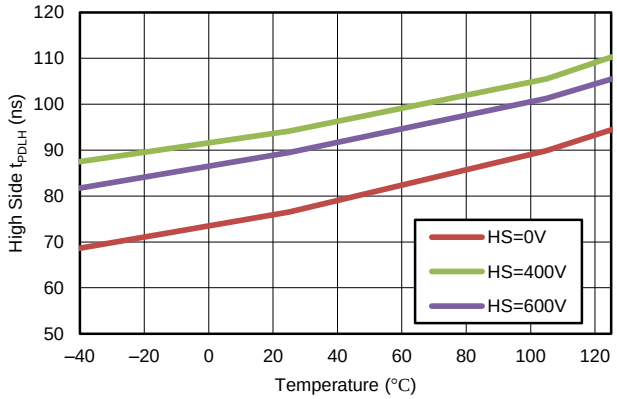


Figure 8. High-Side, Turn-On Propagation Delay vs HS

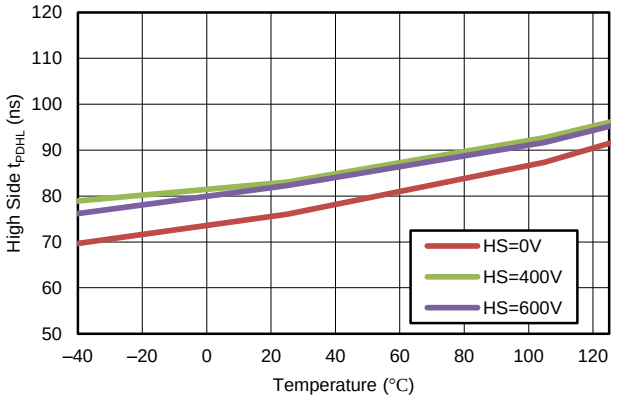


Figure 9. High-Side, Turn-Off Propagation Delay vs HS

Typical Characteristics (continued)

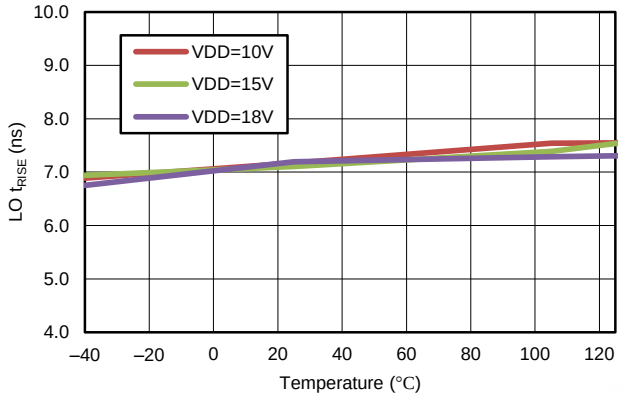


Figure 10. LO Rise Time with 1000-pF Load vs Temperature

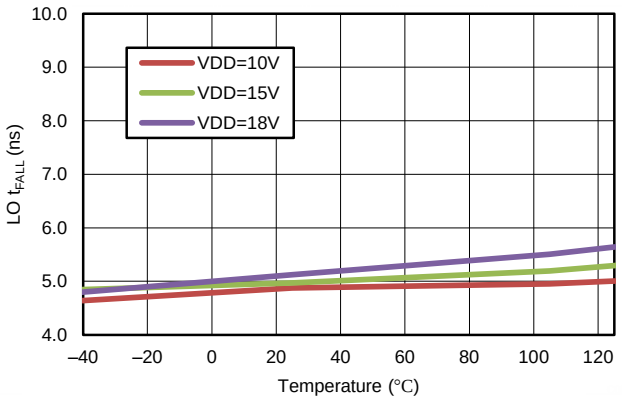


Figure 11. LO Fall Time with 1000-pF Load vs Temperature

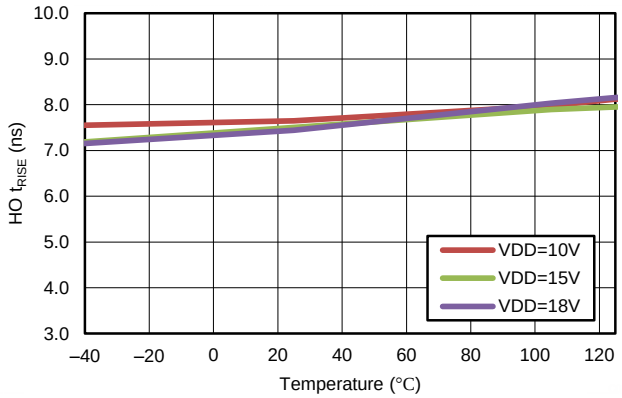


Figure 12. HO Rise Time with 1000-pF Load vs Temperature

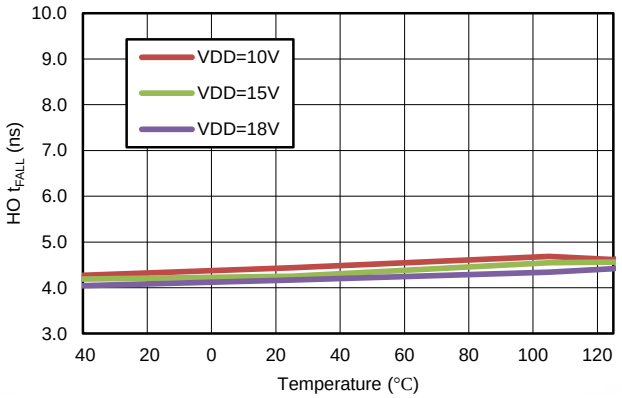


Figure 13. HO Fall Time with 1000-pF Load vs Temperature

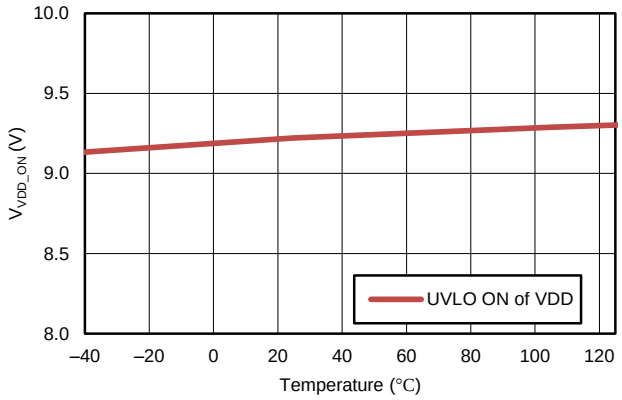


Figure 14. VDD UVLO On Threshold vs Temperature

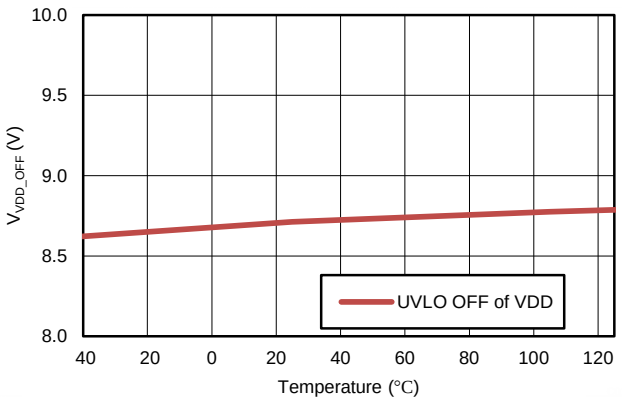


Figure 15. VDD UVLO Off Threshold vs Temperature

Typical Characteristics (continued)

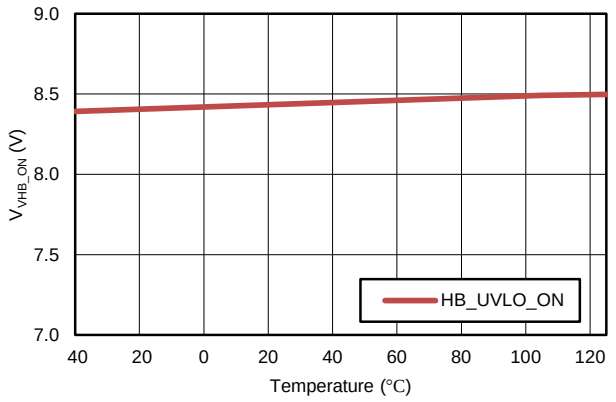


Figure 16. VHB-VHS UVLO On Threshold vs Temperature

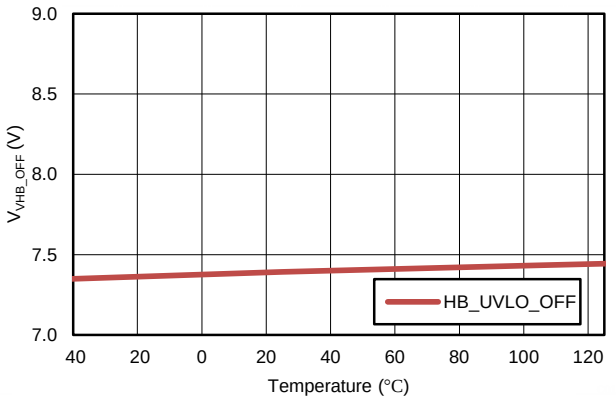


Figure 17. VHB-VHS UVLO Off Threshold vs Temperature

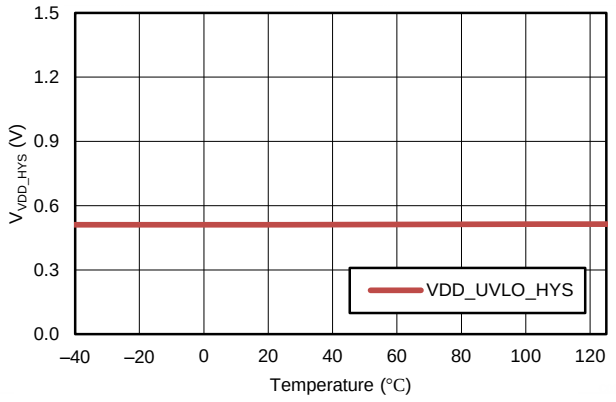


Figure 18. VDD UVLO Hysteresis vs Temperature

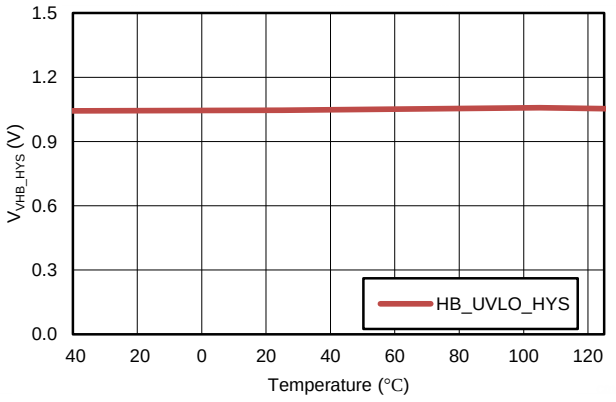


Figure 19. VHB-VHS UVLO Hysteresis vs Temperature

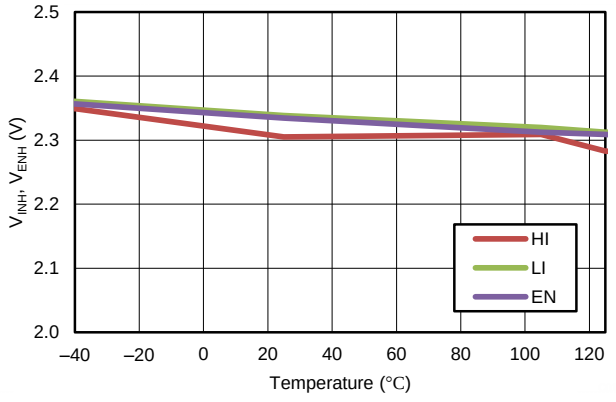


Figure 20. HI/LI/EN Pin High Threshold vs Temperature

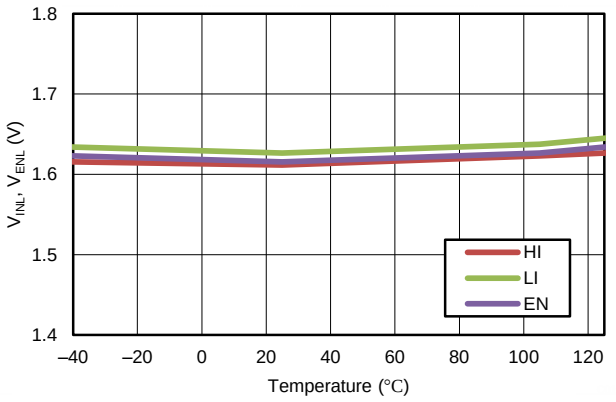


Figure 21. HI/LI/EN Pin Low Threshold vs Temperature

Typical Characteristics (continued)

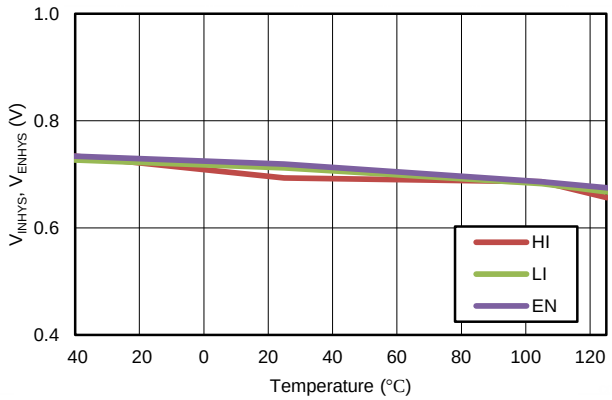


Figure 22. HI/LI/EN Pin Hysteresis vs Temperature

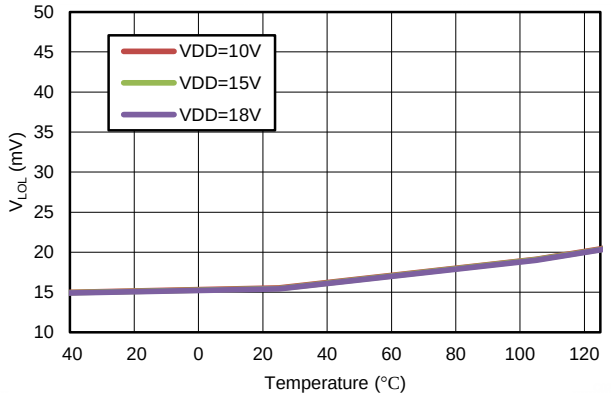


Figure 23. LO Output Low Voltage with 20-mA Load vs Temperature

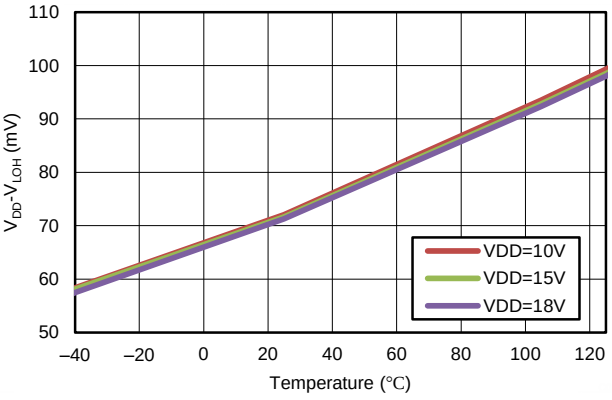


Figure 24. LO Output High Voltage with 20-mA Load vs Temperature

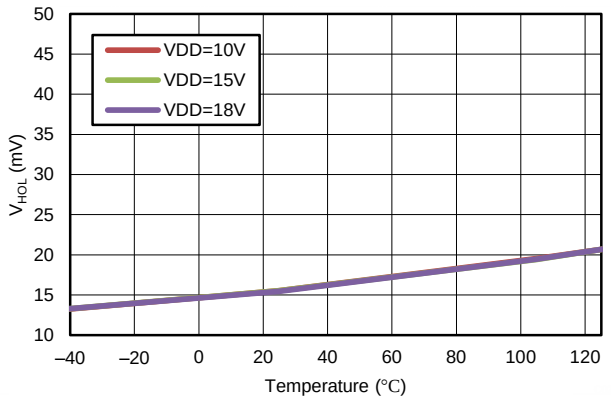


Figure 25. HO Output Low Voltage with 20-mA Load vs Temperature

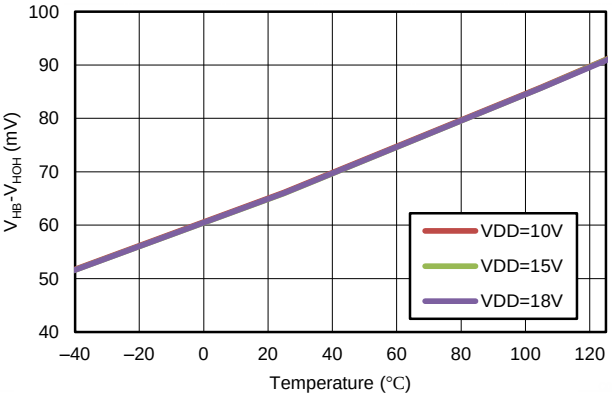


Figure 26. HO Output High Voltage with 20-mA Load vs Temperature

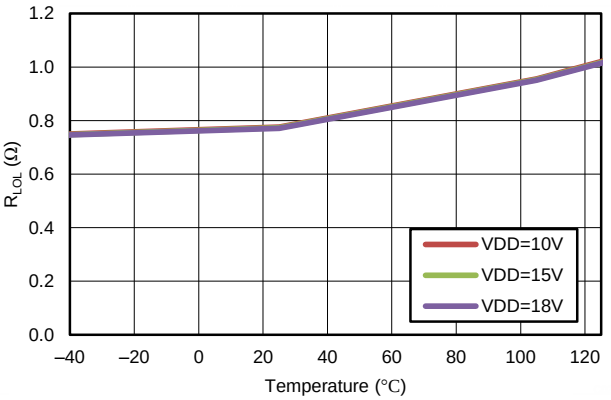


Figure 27. LO Output Pull-Down Resistance vs Temperature

Typical Characteristics (continued)

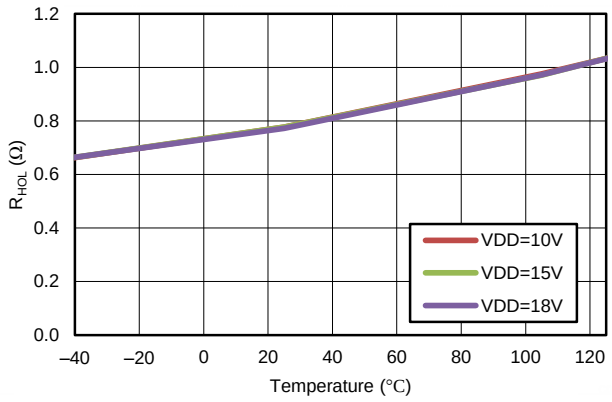


Figure 28. HO Output Pull-Down Resistance vs Temperature

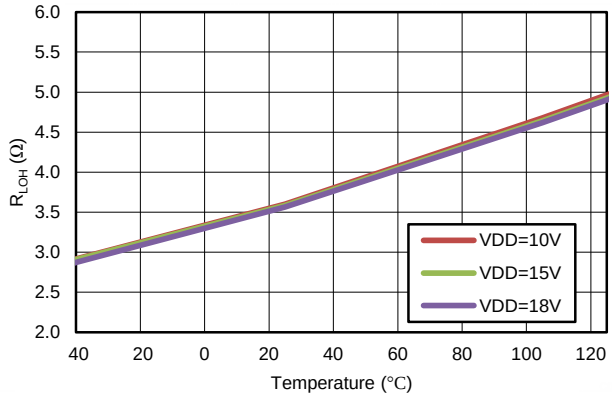


Figure 29. LO Output Pull-Up Resistance vs Temperature

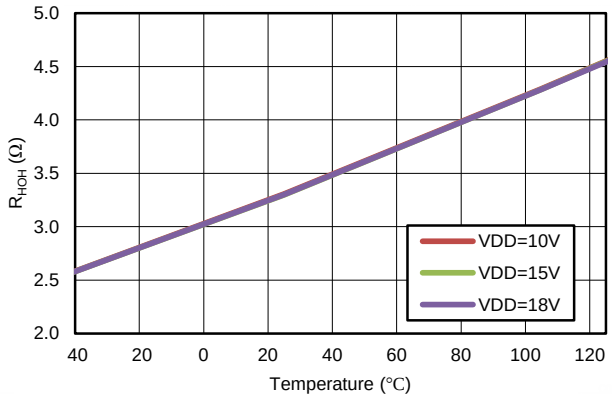


Figure 30. HO Output Pull-Up Resistance vs Temperature

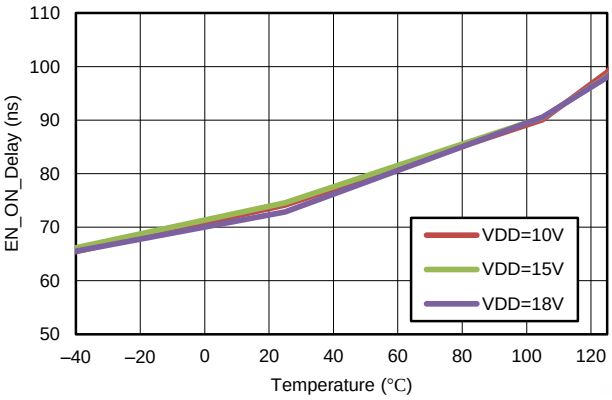


Figure 31. EN ON Response Time vs Temperature

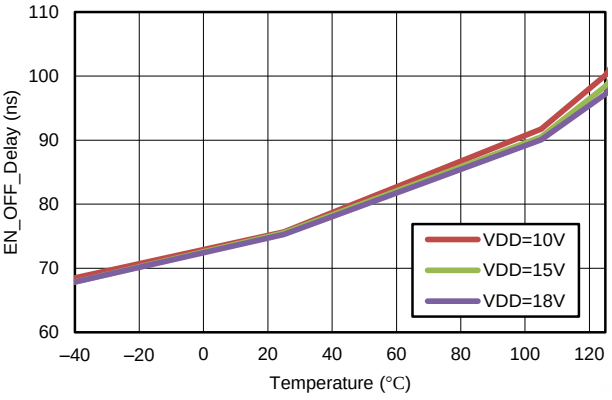


Figure 32. EN OFF Response Time vs Temperature

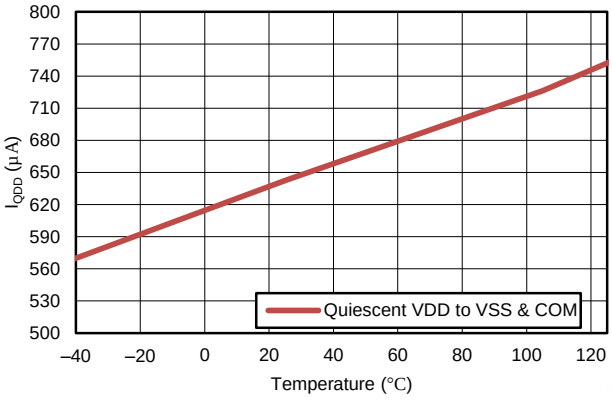


Figure 33. Total Quiescent VDD to VSS and COM Supply Current vs Temperature

Typical Characteristics (continued)

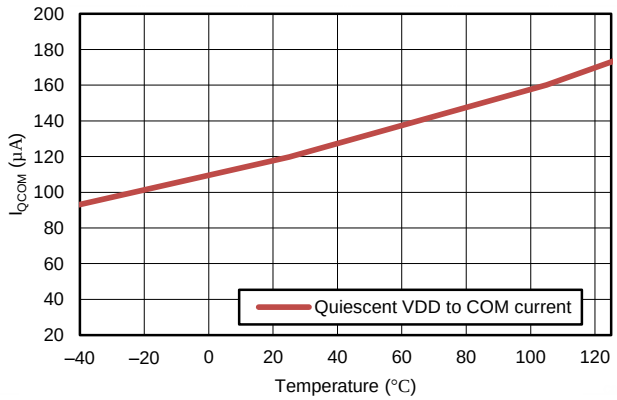


Figure 34. Quiescent VDD to COM Supply Current vs Temperature

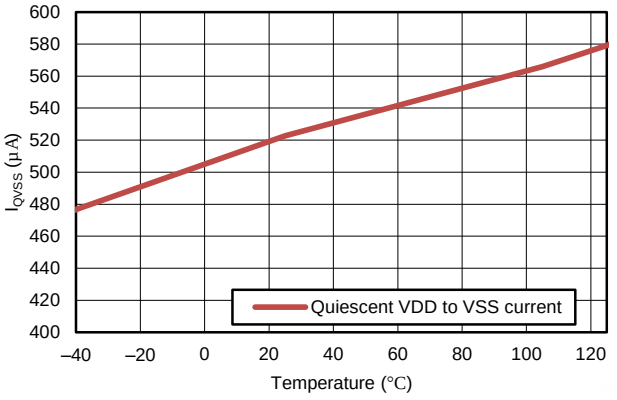


Figure 35. Quiescent VDD to VSS Supply Current vs Temperature

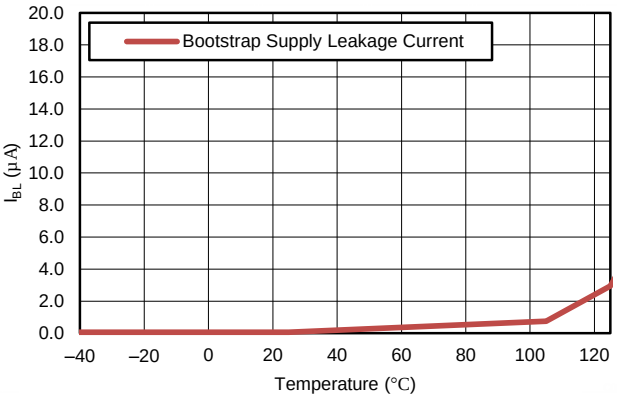


Figure 36. Bootstrap Supply Leakage Current vs Temperature

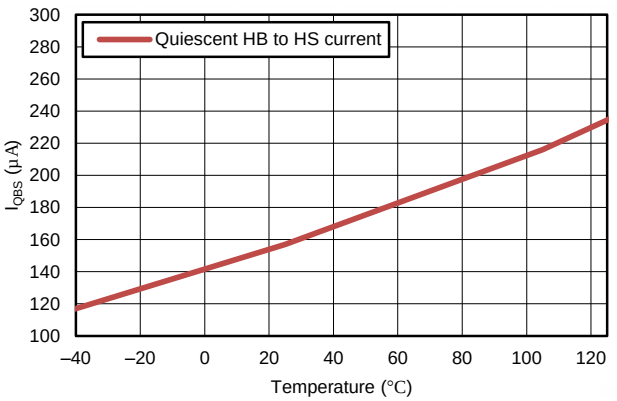


Figure 37. Total Quiescent HB to HS Supply Current

8 Detailed Description

8.1 Overview

High-current, gate-driver devices are required in switching power applications for a variety of reasons. In order to implement fast switching of power devices and reduce associated switching power losses, a powerful gate-driver device is employed between the PWM output of control devices and the gates of the power semiconductor devices. Further, gate-driver devices are indispensable when having the PWM controller device directly drive the gates of the switching devices is sometimes not feasible. In the case of digital power supply controllers, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which is not capable of effectively turning on a power switch.

In bridge topologies, like hard-switch half bridge, hard-switch full bridge, half-bridge and full-bridge LLC, phase-shift full bridge, 2-transistor forward, the source and emitter pin of the top-side power MOSFET and IGBT switch is referenced to a node whose voltage changes dynamically; that is, not referenced to a fixed potential, so floating-driver devices are necessary in these topologies.

The UCC27714 is a high-side and low-side driver dedicated for offline AC-to-DC power supplies and inverters. The high side is a floating driver that can be biased effectively using a bootstrap circuit, and can handle up to 600-V. The driver includes an enable and disable function, and can be used with 100% duty cycle as long as HB-HS can be above UVLO of the high side.

The device features industry best-in-class propagation delays and delay matching between both channels aimed at minimizing pulse distortion in high-frequency switching applications. Each channel is controlled by its respective input pins (HI and LI), allowing full and independent flexibility to control on and off state of the output. The UCC27714 includes protection features wherein the outputs are held low when inputs are floating or when the minimum input pulse width specification is not met. The driver inputs are CMOS and TTL compatible for easy interface to digital power controllers and analog controllers alike. An optional enable and disable function is included in Pin 4 of the UCC27714. The pin is internally pulled to VDD for active-high logic and can be left open (NC) for standard operation when outputs are enable by default. If the pin is pulled to GND, then outputs are disabled.

8.2 Functional Block Diagram

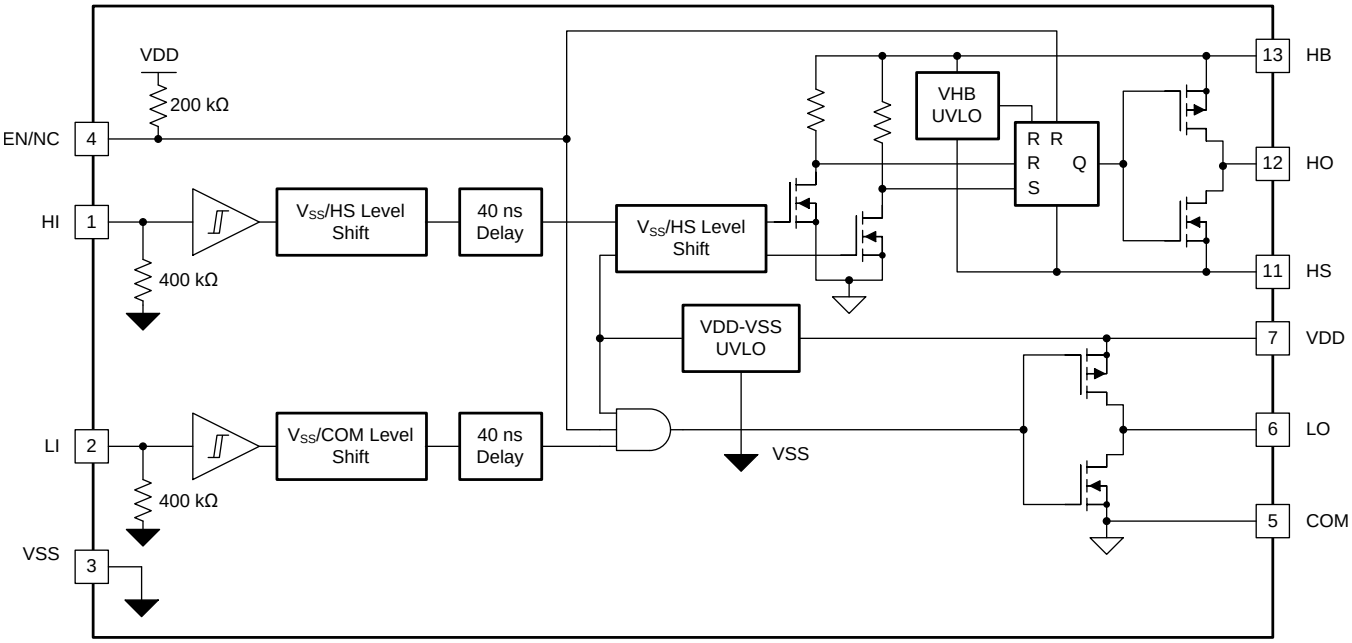


Figure 38. UCC27714 Block Diagram

8.3 Feature Description

8.3.1 VDD and Under Voltage Lockout

The UCC27714 has an internal under voltage-lockout (UVLO) protection feature on the supply circuit blocks between VDD and VSS pins, as well as between HB and HS pins. When VDD bias voltage is lower than the $V_{VDD(on)}$ threshold at device start-up or lower than $V_{VDD(off)}$ after start-up, the VDD UVLO feature holds both the LO and HO outputs LOW, regardless of the status of the HI and LI inputs. On the other hand, if HB-HS bias supply voltage is lower than the $V_{VHB(on)}$ threshold at start-up or $V_{VHB(off)}$ after start-up, the HB-HS UVLO feature only holds HO to LOW, regardless of the status of the HI. The LO output status is not affected by the HB-HS UVLO feature (see Table 1 and Table 2). This allows the LO output to turn-on and re-charge the HB-HS capacitor using the boot-strap circuit and thus allows HB-HS bias voltage to surpass the $V_{VHB(on)}$ threshold.

Both the VDD and VHB UVLO protection functions are provided with a hysteresis feature. This hysteresis prevents chatter when there is ground noise from the power supply. Also this allows the device to accept a small drop in the bias voltage which is bound to happen when the device starts switching and quiescent current consumption increases instantaneously, as well as when the boot-strap circuit charges the HB-HS capacitor during the first instance of LO turn-on causing a drop in VDD voltage.

The UVLO circuit of VDD-VSS and HB-HS in UCC27714 generate internal signals to enable/disable the outputs after UVLO_ON/UVLO_OFF thresholds are crossed respectively (please refer to Figure 39). Design considerations indicate that the UVLO propagation delay before the outputs are enabled and disabled can vary from 10 µs to 70 µs.

Special attention must be paid to the situation when the VDD-VSS voltage drops rapidly, during abnormal condition tests such as pin-to-pin shorting. If VDD-VSS voltage drops from $VDD_{(OFF)}$ to a 4-V level in a time that is less than the propagation delay, then there is a chance for the HO and LO outputs to be latched in the incumbent state prior to the UVLO incident. For UVLO_OFF logic block to be effective in turning off the outputs, the VDD-VSS bias voltage must be at least 4 V. Hence, it is recommended that VDD pin voltage is not allowed to dip from $VDD_{(OFF)}$ to 4 V in 70 µs or less.

Table 1. VDD UVLO Feature Logic Operation

CONDITION (VHB-VHS>$V_{VHB, ON}$ FOR ALL CASES BELOW)	HI	LI	HO	LO
VDD-VSS < $V_{VDD(on)}$ during device start up	H	L	L	L
VDD-VSS < $V_{VDD(on)}$ during device start up	L	H	L	L
VDD-VSS < $V_{VDD(on)}$ during device start up	H	H	L	L
VDD-VSS < $V_{VDD(on)}$ during device start up	L	L	L	L
VDD-VSS < $V_{VDD(off)}$ after device start up	H	L	L	L
VDD-VSS < $V_{VDD(off)}$ after device start up	L	H	L	L
VDD-VSS < $V_{VDD(off)}$ after device start up	H	H	L	L
VDD-VSS < $V_{VDD(off)}$ after device start up	L	L	L	L

Table 2. VHB UVLO Feature Logic Operation

CONDITION (VDD-VSS > $V_{VDD,ON}$ FOR ALL CASES BELOW)	HI	LI	HO	LO
VHB-VHS < $V_{VHB(on)}$ during device start up	H	L	L	L
VHB-VHS < $V_{VHB(on)}$ during device start up	L	H	L	H
VHB-VHS < $V_{VHB(on)}$ during device start up	H	H	L	H
VHB-VHS < $V_{VHB(on)}$ during device start up	L	L	L	L
VHB-VHS < $V_{VHB(off)}$ after device start up	H	L	L	L
VHB-VHS < $V_{VHB(off)}$ after device start up	L	H	L	H
VHB-VHS < $V_{VHB(off)}$ after device start up	H	H	L	H
VHB-VHS < $V_{VHB(off)}$ after device start up	L	L	L	L

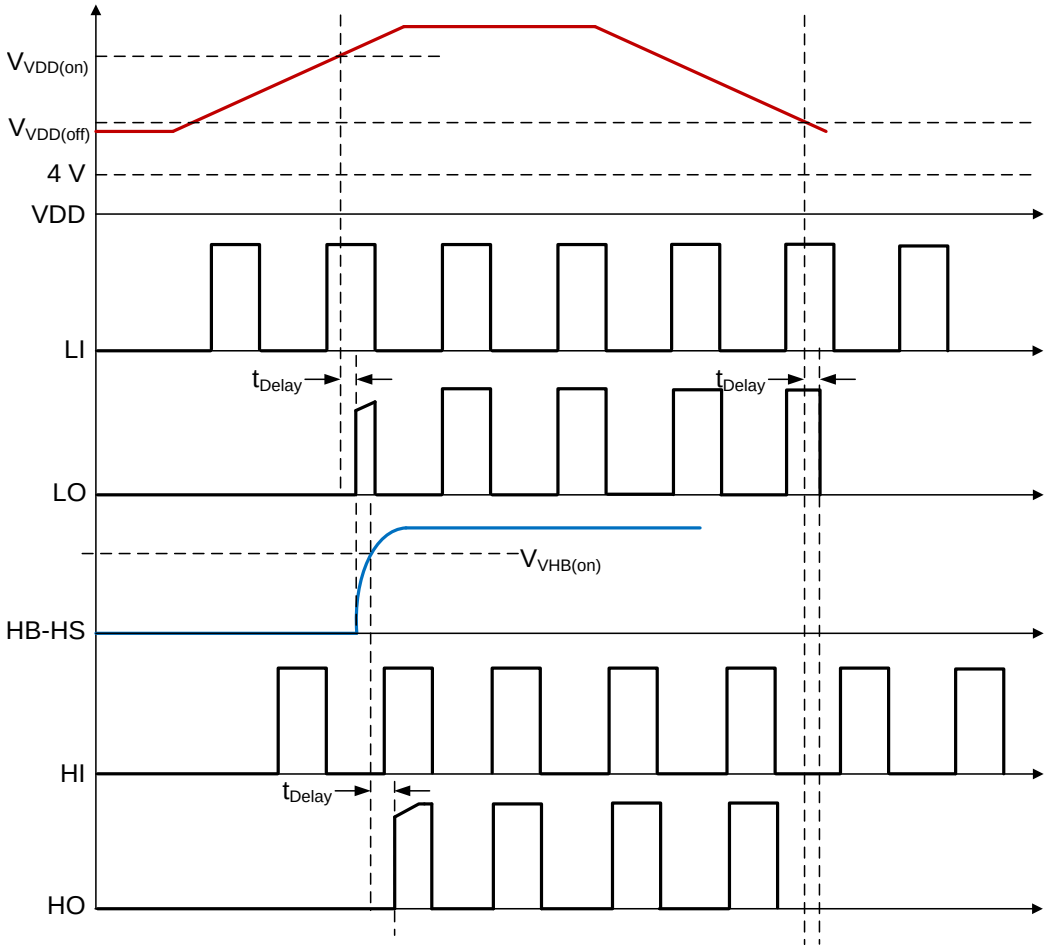


Figure 39. Power-Up Driver

8.3.2 Input and Output Logic Table

UCC27714 features independent inputs, HI and LI, for controlling the state of the outputs, HO and LO, respectively. The device does not include internal cross-conduction prevention logic and allows both HO and LO outputs to be turned on simultaneously (refer to Table 3). This feature allows it to be used topologies such as 2-transistor forward.

Table 3. Input/Output Logic Table (1)
(Assuming no UVLO fault condition exists for VDD and VHB)

EN/NC	HI	LI	HO	LO
H	L	L	L	L
H	L	H	L	H
H	H	L	H	L
H	H	H	H	H
L	Any	Any	L	L
Any	×	×	L	L
×	L	L	L	L
×	L	H	L	H
×	H	L	H	L
×	H	H	H	H

(1) × = floating condition

8.3.3 Input Stage

The input pins of UCC27714 are based on a TTL and CMOS compatible input-threshold logic that is independent of the VDD supply voltage. With typical high threshold (V_{INH}) of 2.3 V and typical low threshold (V_{INL}) of 1.6 V, along with very little temperature variation as summarized in Figure 20 and Figure 21, the input pins are conveniently driven with logic level PWM control signals derived from 3.3-V and 5-V digital power-controller devices. Wider hysteresis (typically 0.7 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. UCC27714 also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature.

The UCC27714 includes an important feature: wherein, whenever any of the input pins is in a floating condition, the output of the respective channel is held in the low state. This is achieved using GND pull-down resistors on all the input pins (HI, LI), the input impedance of the input pins (HI, LI) is 400-kΩ typically, as shown in the device block diagrams.

The UCC27714 input pins are capable of sustaining voltages higher than the bias voltage applied on the VDD pin of the device, as long as the absolute magnitude is less than the recommended operating condition's maximum ratings. This features offers the convenience of driving the PWM controller at a higher VDD bias voltage than the UCC27714 helping to reduce gate charge related switching losses. This capability is envisaged in UCC27714 by way of two ESD diodes tied back-to-front as shown in Figure 40.

Additionally, the input pins are also capable of sustaining negative voltages below VSS, as long as the magnitude of the negative voltage is less than the recommended operating condition minimum ratings. A similar diode arrangement exists between the input pins and VSS as illustrated in Figure 40.

The input stage of each driver must be driven by a signal with a short rise or fall time. This condition is satisfied in typical power supply applications, when the input signals are provided by a PWM controller or logic gates with fast transition times. With a slow changing input voltage, the output of driver may switch repeatedly at a high frequency. While the wide hysteresis offered in UCC27714 definitely alleviates this concern over most other TTL input threshold devices, extra care is necessary in these implementations. If limiting the rise or fall times to the power device is the primary goal, then an external resistance is highly recommended between the output of the driver and the power device. This external resistor has the additional benefit of reducing part of the gate-charge related power dissipation in the gate-driver device package and transferring it into the external resistor itself. If an RC filter is to be added on the input pins for reducing the impact of system noise and ground bounce, the time constant of the RC filter must be 20 ns or less, for example, 50 Ω with 220 pF is an acceptable choice.

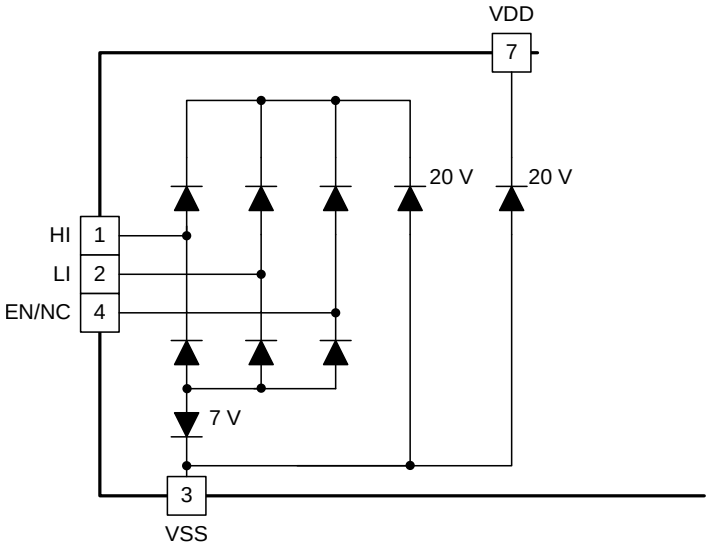


Figure 40. Diode Structure of Input Stage

8.3.4 Output Stage

The UCC27714 device output stage features a unique architecture on the pull up structure which delivers the highest peak-source current when it is most needed during the Miller plateau region of the power-switch turn on transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-Channel MOSFET and an additional N-Channel MOSFET in parallel. The function of the N-Channel MOSFET is to provide a brief boost in the peak sourcing current enabling fast turn on. This is accomplished by briefly turning-on the N-Channel MOSFET during a narrow instant when the output is changing state from low to high.

The R_{OH} parameter (see Electrical Characteristics) is a DC measurement and it is representative of the on-resistance of the P-Channel device only. This is because the N-Channel device is held in the off state in DC condition and is turned on only for a narrow instant when output changes state from low to high.

NOTE

The effective resistance of UCC27714 pull-up stage during the turn-on instant is much lower than what is represented by R_{OH} parameter.

The pull-down structure in UCC27714 is simply composed of a N-Channel MOSFET. The R_{OL} parameter (see Electrical Characteristics), which is also a DC measurement, is representative of the impedance of the pull-down stage in the device.

Each output stage in UCC27714 is capable of supplying 4-A peak source and 4-A peak sink current pulses. The output voltage swings between (VDD and COM) / (HB and HS) providing rail-to-rail operation, thanks to the MOS-out stage which delivers very low drop-out. The low drop-out voltage is summarized in Figure 23, Figure 24, Figure 25 and Figure 26

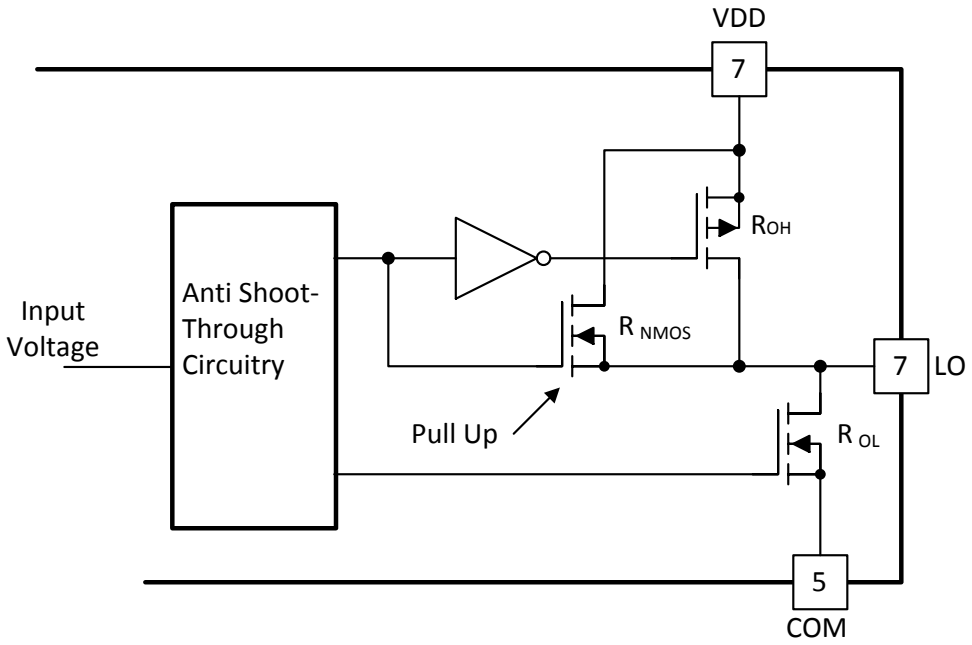


Figure 41. Output Stage Structure

8.3.5 Level Shift

The level shift circuit (refer to the Functional Block Diagram) is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). It is a pulsed generated level shifter. With an input signal the pulse generator generates "on" pulses based on the rising edge of the signal and "off" pulses based on the falling edge. On pulses and off pulses turn on each branch of the level shifter so that current flows in each branch to generate different voltages, which is transferred to the set and reset signal in the high side. The signal is rebuilt by the RS latch in the high side domain. The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver. The delay matching of UCC27714 is summarized in Figure 6 and Figure 7.

The level shifter in UCC27714 offers best-in-class capability while operating under negative voltage conditions on HS pin. The level shifter is able to transfer signals from the HI input to HO output with only 4-V headroom between HB and COM. Refer to Operation Under Negative HS Voltage Condition for detailed explanations.

8.3.6 Low Propagation Delays and Tightly Matched Outputs

The UCC27714 features a best in class, 90-ns (typical) propagation delay (refer to Figure 2, Figure 3, Figure 4 and Figure 5) between input and output in high voltage 600-V driver, which goes to offer the lowest level of pulse-transmission distortion available in the industry for high frequency switching applications.

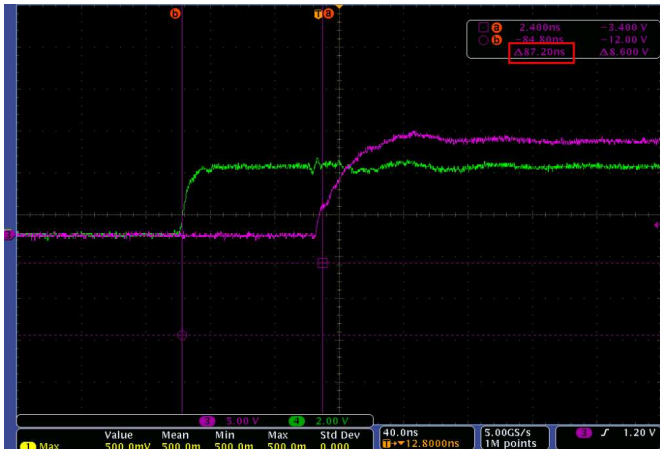


Figure 42. Turn-On Propagation Delay

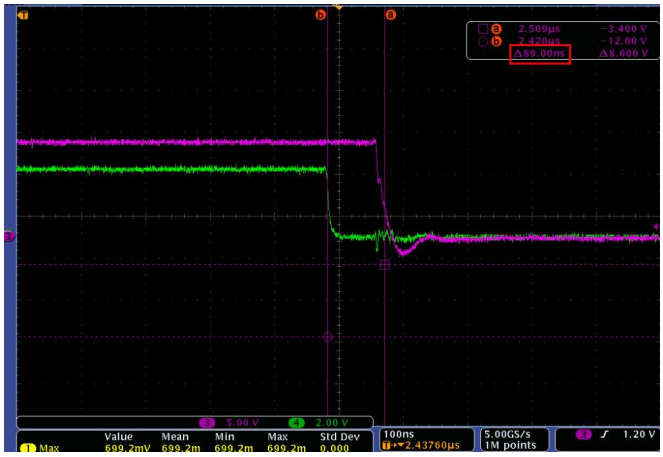


Figure 43. Turn-Off Propagation Delay

8.3.7 Parasitic Diode Structure in UCC27714

Figure 44 illustrates the multiple parasitic diodes involved in the ESD protection components of UCC27714 device. This provides a pictorial representation of the absolute maximum rating for the device.

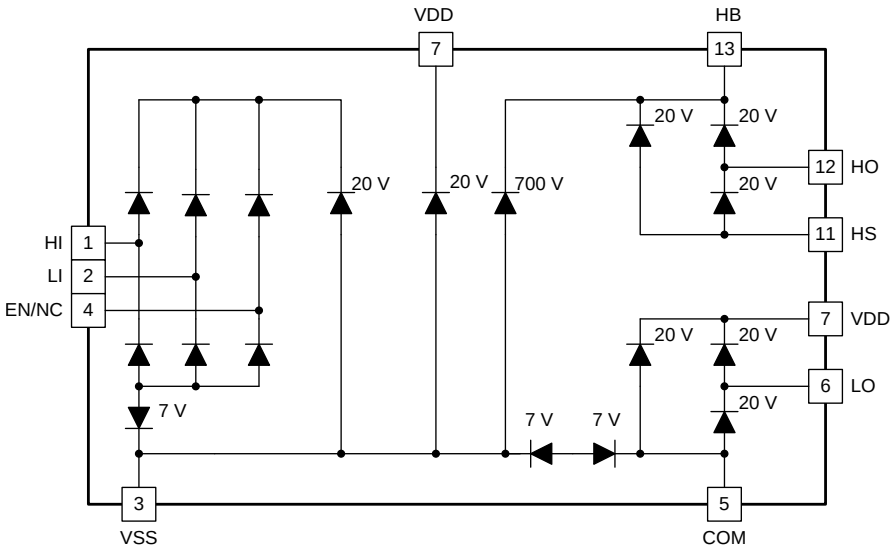


Figure 44. ESD Structure

8.4 Device Functional Modes

8.4.1 Enable Function

The enable function is an extremely beneficial feature in applications where the DC-to-DC controller is located on the secondary side, which is very common with digital controllers. In these applications, it is easy to turn off the driver signal in a very short time when critical faults such as primary-side overcurrent occurs. The Enable Function response time is typically around 80 ns, refer to Figure 31, Figure 32 and Figure 45.

The enable pin controls both the high-side and low-side driver-channel operation. The enable pin is based on a non-inverting configuration (active-high operation). Thus, when EN pin is driven high the driver is enabled and when EN pin is driven low the driver outputs are low. The EN pin is internally pulled up to VDD using 200-kΩ, pull-up resistor as a result of which the outputs of the device are enabled in the default state. The EN pin is left floating or Not Connected (N/C) for standard operation, where the enable feature is not needed. Care must be taken not to connect the EN pin to ground, which permanently disables the device. Like the input pins, the enable pin is also based on a TTL and CMOS compatible input-threshold logic that is independent of the supply voltage and is effectively controlled using logic signal from 3.3-V and 5-V microcontrollers. The UCC27714 also features tight control of the enable-function-threshold voltage levels which eases system design considerations and ensures stable operation across temperature (refer to Figure 20 and Figure 21).

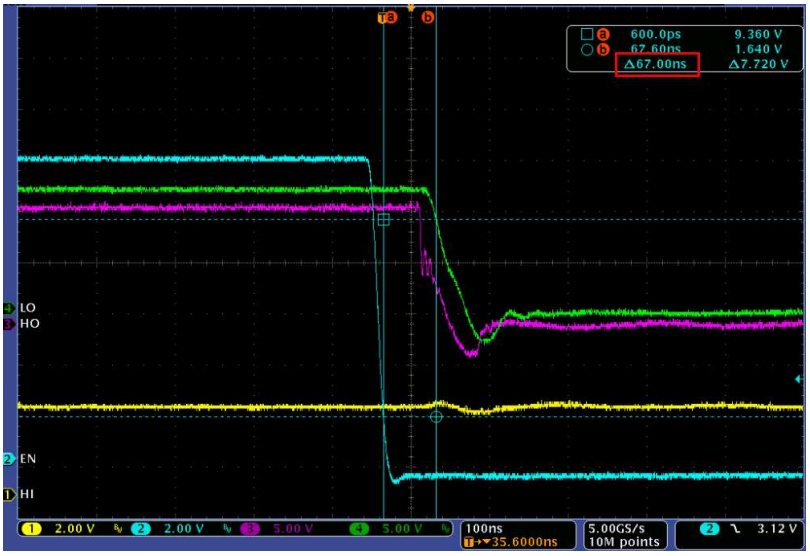


Figure 45. EN Function Response Time

Device Functional Modes (continued)

8.4.2 Minimum Input Pulse Operation

The UCC27714 device has a minimum turn-on, turn-off pulse transfer function to the output pin from the input pin. This function ensures UCC27714 is in the correct state when the input signal is very narrow. The function is summarized in Figure 46 and Figure 47. The 100 ns shown in Figure 46 and Figure 47 is ensured by design.

The t_{ON} and t_{OFF} parameters in the electrical table are characterized by applying a 100-ns wide input pulses and monitoring for a corresponding change of state in the outputs.

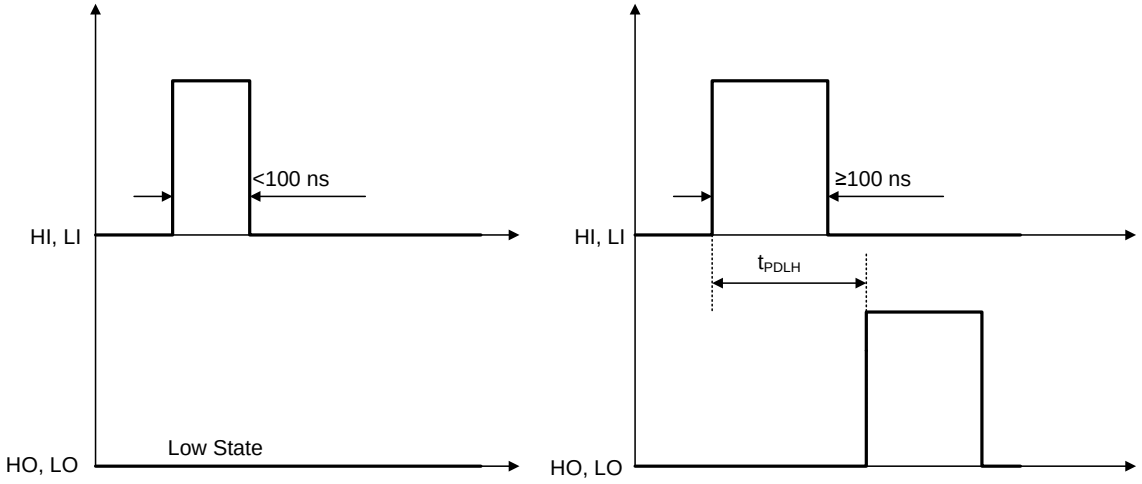


Figure 46. Minimum Turn-On Pulse

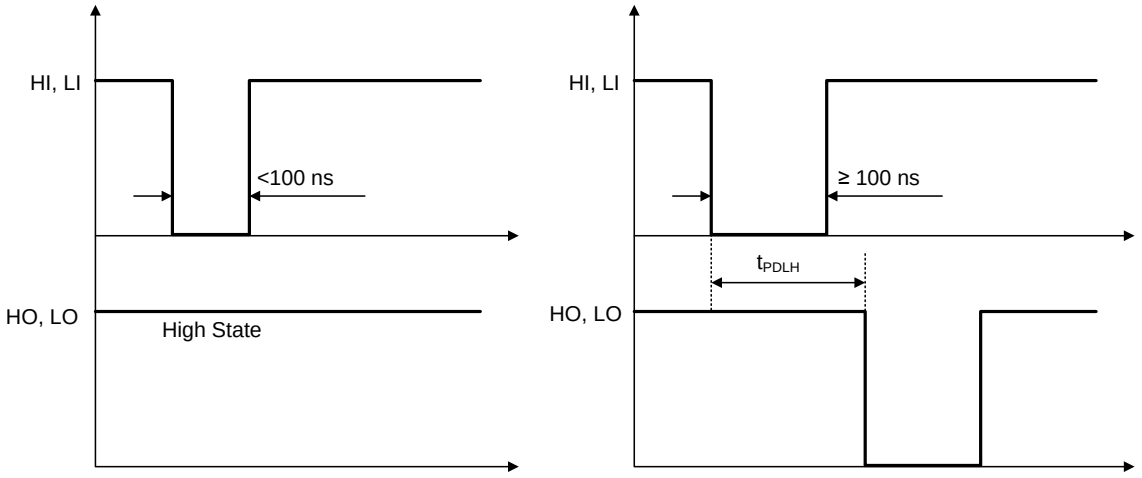


Figure 47. Minimum Turn-Off Pulse

Device Functional Modes (continued)

8.4.3 Operation with HO and LO Outputs High Simultaneously

The UCC27714 does not have cross-conduction prevention logic, which is a feature that does not allow both the high-side and low-side outputs to be in high state simultaneously. In some power supply topologies, such as two-transistor forward, it is required for both the high-side and low-side power switches to be turned on simultaneously. The UCC27714 can handle both HO and LO high condition at same time as long as there are no bias supply UVLO fault conditions present. Figure 48 illustrates the mode of operation where both HO and LO outputs are in high state.

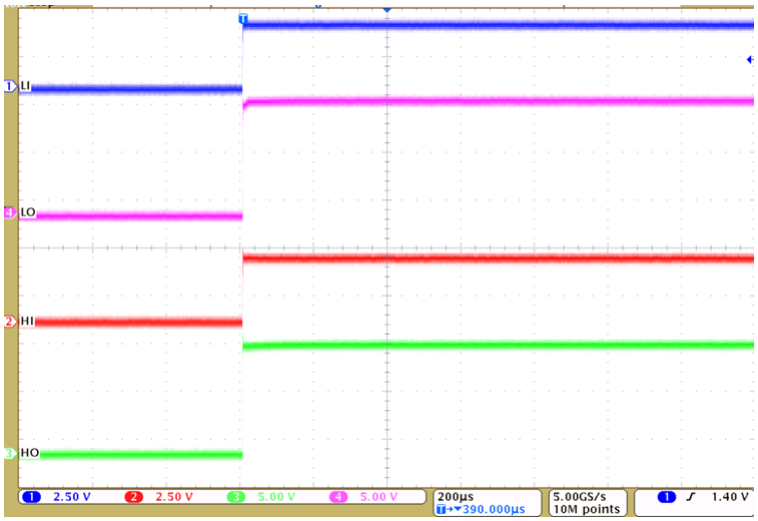


Figure 48. Simultaneously Supported HO and LO High State

The circuit in Figure 49 shows a two-transistor forward converter circuit driven by the UCC27714. This circuit requires both outputs to be high or low simultaneously. The bootstrap capacitor would be charged with LO high state only (HO low). As this would decrease overall system efficiency two additional diode and two additional transistors are required to charge the bootstrap capacitor during LO and HO low period.

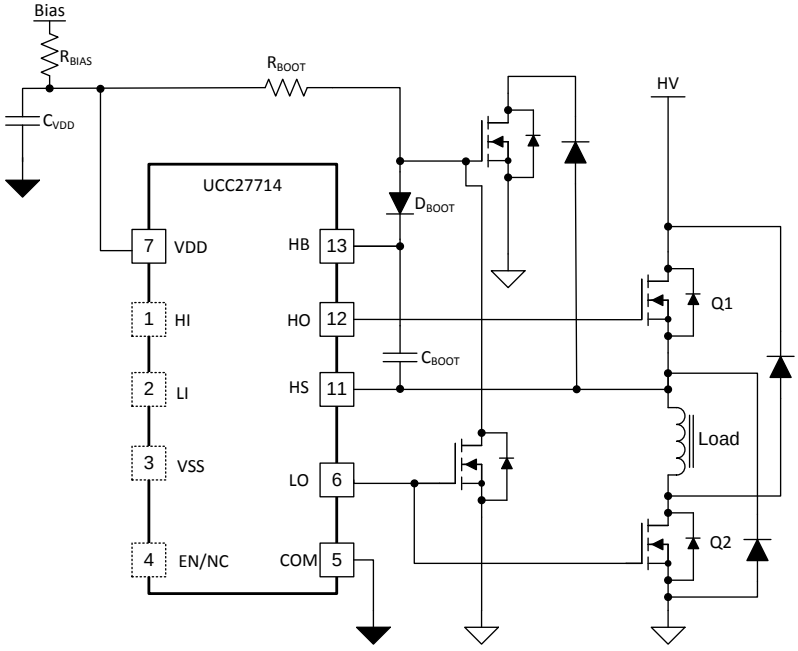


Figure 49. Two-Transistor Forward Converter Circuit

Device Functional Modes (continued)

8.4.4 Operation Under 100% Duty Cycle Condition

The UCC27714 allows constant on or constant off operation (0% and/or 100% duty cycle) as long as the VDD and VHB bias supplies are maintained above the UVLO thresholds. This is a challenge when boot-strap supplies are used for VHB. However, when a dedicated bias supply is used, constant on or constant off conditions can be supported, refer to Figure 48.

8.4.5 Operation Under Negative HS Voltage Condition

A typical half-bridge configuration with UCC27714 is shown in Figure 50. There are parasitic inductances in the power circuit from die bonding and pinning in QT/QB and PCB tracks of power circuit, the parasitic inductances are labeled $L_{K1,2,3,4}$.

During switching of HS caused by turning off HO, the current path of power circuit is changed to current path 2 from current path 1. This is known as current commutation. The current across L_{K3}, L_{K4} and body diode of QB pulls HS lower than COM, like shown in the waveform in Figure 50. The negative voltage of HS with respect to COM causes a logic error of HO if the driver cannot handle negative voltage of HS. However, the UCC27724 offers robust operation under these conditions of negative voltage on HS.

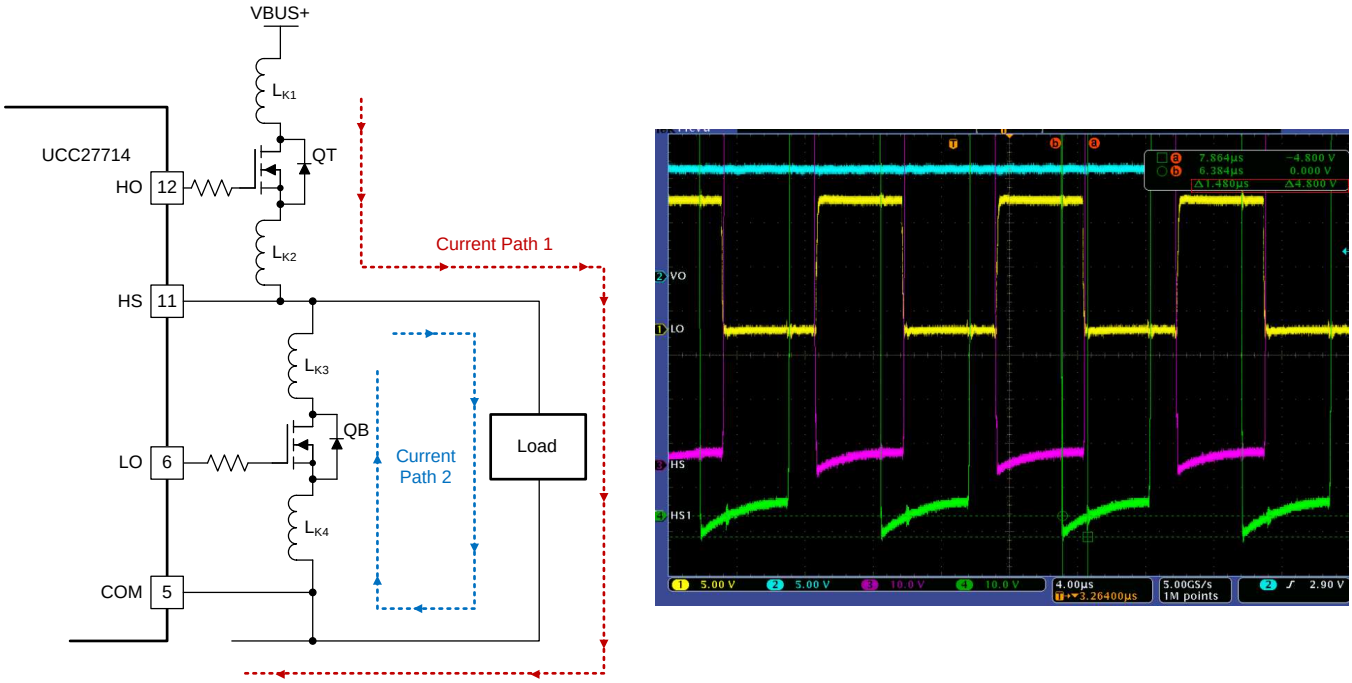


Figure 50. HS Negative Voltage In Half-Bridge Configuration

Device Functional Modes (continued)

The level shifter circuit is respect to COM (refer to Functional Block Diagram), the voltage from HB to COM is the supply voltage of level shifter. Under the condition of HS is negative voltage with respect to COM, the voltage of HB-COM is decreased, as shown in Figure 51. There is a minimum operational supply voltage of level shifter, if the supply voltage of level shifter is too low, the level shifter cannot pass through HI signal to HO. The minimum supply voltage of level shifter of UCC27714 is 4 V, so the recommended HS specification is dependent on HB-HS. The specification of recommended HS is –8 V at HB – HS = 12 V.

In general, HS can operate until -8 V when HB – HS = 12 V as the ESD structure in Figure 44 allows a maximum voltage difference of 20 V between both pins. If HB-HS voltage is different, the minimum HS voltage changes accordingly.

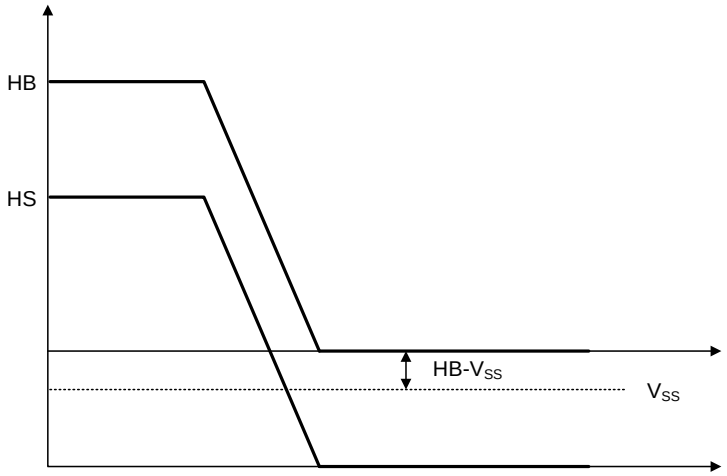


Figure 51. Level Shifter Supply Voltage with Negative HS

NOTE

Logic operational for HS of –8 V to 600 V at HB – HS = 12 V

Device Functional Modes (continued)

The capability of a typical UCC27714 device to operate under a negative voltage condition in HS pin is reported in Figure 53. The test method and typical failure mode are shown in Figure 52, where the HO output can be seen to flip from low to high, even while the HI input is held low.

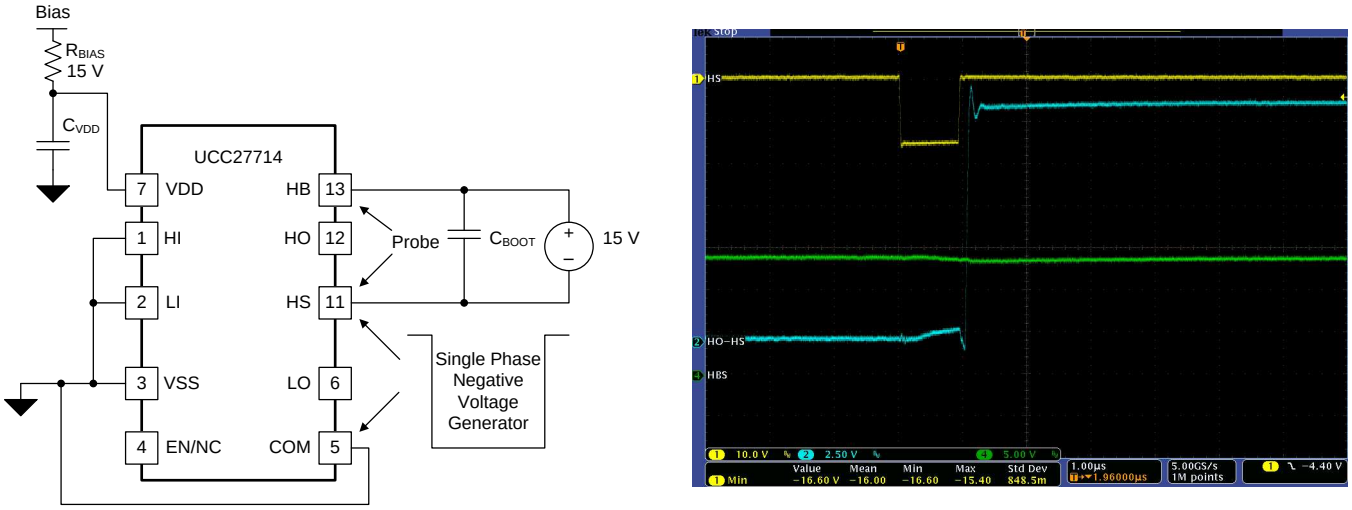


Figure 52. Negative Voltage Test Method and Typical Failure Mode

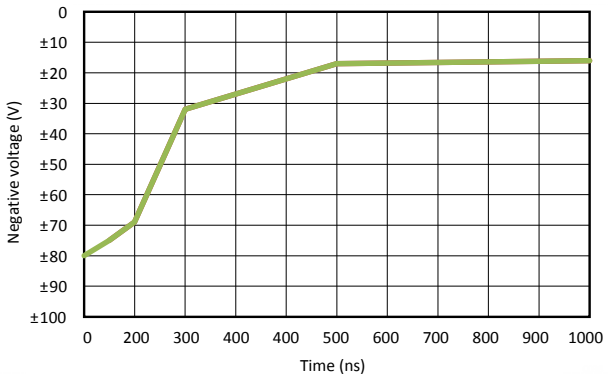


Figure 53. Negative Voltage Chart Time vs Negative Voltage

9 Application and Implementation

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

To effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation will be often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability.

Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

9.2 Typical Application

The circuit in Figure 54 shows two UCC27714 in a phase shifted full bridge setup converting 370 V – 410 V DC into 12 V while driving up to 50-A output current. The UCC27524A drives the secondary side. All gate drivers are controlled by the UCC28950. The leading leg is shown in detail.

For more information, please refer to UCC27714EVM-551.

Typical Application (continued)

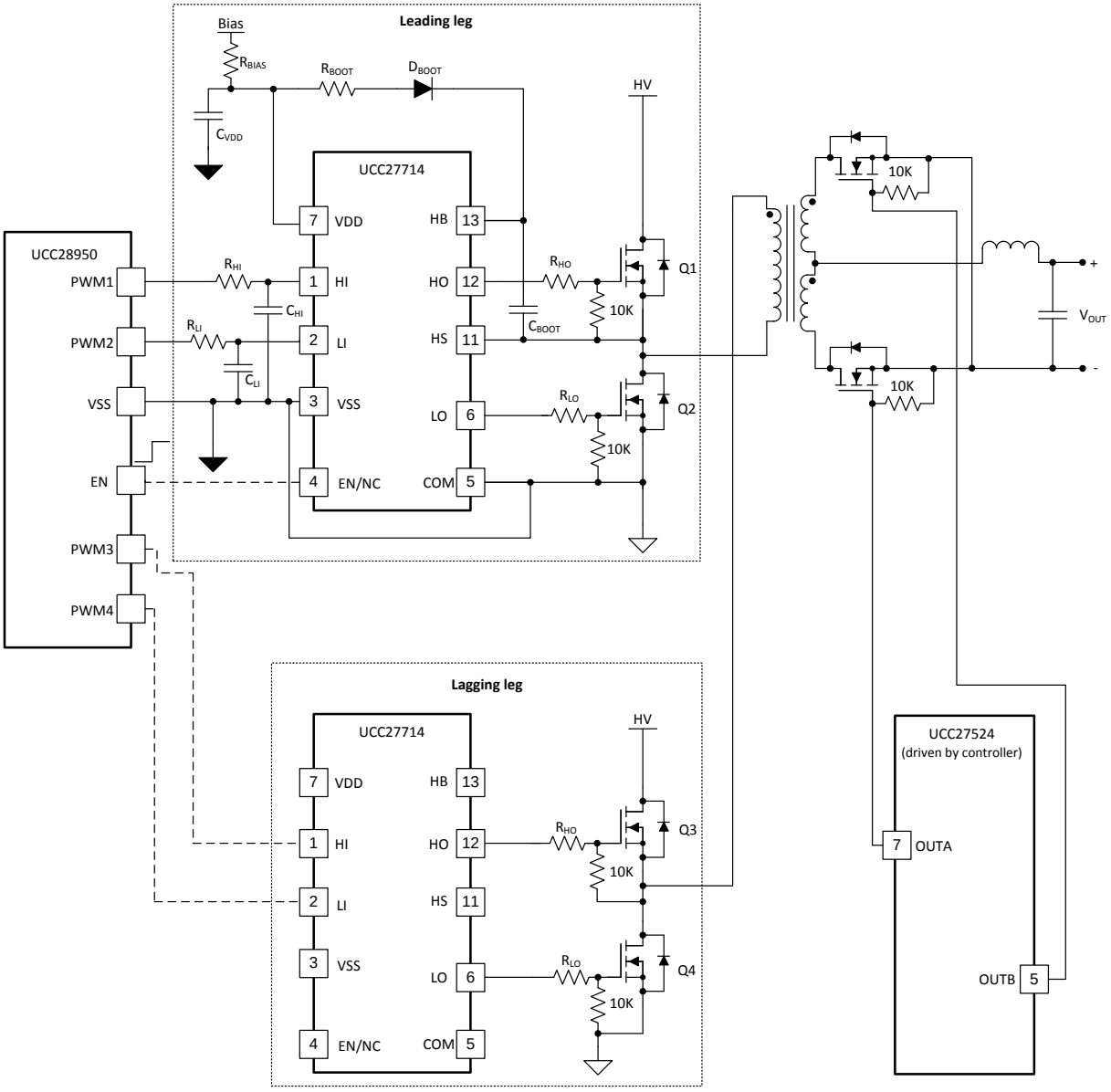


Figure 54. Typical Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

Table 4 shows the design requirements for a 600-W power supply used as an example to illustrate the design process.

Table 4. UCC27714 Design Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
	DC input voltage range		370	390	410	V
$I_{IN(max)}$	Maximum input current	V_{IN}= 370 V_{DC} to 410 V_{DC}			2	A
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage	V_{IN} = 370 V_{DC} to 410 V_{DC}	11.4	12	12.6	V
I_{OUT}	Output current	V_{IN} = 370 V_{DC} to 410 V_{DC}			50	A
P_{OUT}	Continuous output power	V_{IN} = 370 V_{DC} to 410 V_{DC}			600	W

9.2.2 Detailed Design Procedure

This procedure outlines the steps to design a 600-V high-side, low-side gate driver with 4-A source and 4-A sink current capability, targeted to drive power MOSFETs or IGBTs using the UCC27714. Refer to Figure 54 for component names and network locations. For additional design help see the UCC27714EVM-551 User Guide, SLUUB02.

9.2.2.1 Selecting HI and LI Low Pass Filter Components (R_{HI}, R_{LI}, C_{HI}, C_{LI})

A RC filter should be added between PWM controller and input pin of UCC27714 to filter the high frequency noise, like R_{HI}/C_{HI} and R_{LI}/C_{LI} which shown in Figure 54. The recommended values of the RC filter is refer to Equation 1 and Equation 2:

$$R_{HI} = R_{LI} = 51\,\Omega \tag{1}$$

$$C_{HI} = C_{LI} = 220\text{ pF} \tag{2}$$

9.2.2.2 Selecting Bootstrap Capacitor (C_{BOOT})

The bootstrap capacitor should be sized to have more than enough energy to drive the gate of FET Q1 high, without depleting the boot capacitor more than 10%. A good rule of thumb is size C_{BOOT} to be at least 10 times; as large as the equivalent FET gate capacitance (C_g).

C_g will have to be calculated based voltage driving the high side FET's gate (V_{Q1g}) and knowing the FET's gate charge (Q_g). V_{Q1g} is approximately the bias voltage supplied to VDD less the forward voltage drop of the boost diode (V_{DBOOT}). In this design example, the estimated V_{Q1g} was approximately 11.4V

$$V_{Q1g} \approx V_{VDD} - V_{DBOOT} = 12\text{ V} - 0.6\text{ V} = 11.4\text{ V} \tag{3}$$

The FET used in this example had a specified Q_g of 87 nC. Based on Q_g and V_{Q1g} the calculated C_g was 7.63 nF.

$$C_g = \frac{Q_g}{V_{Q1g}} = \frac{87\text{ nC}}{11.4\text{ V}} \approx 7.63\text{ nF} \tag{4}$$

Once C_g is estimated C_{BOOT} should be sized to be at least 10 times larger than C_g.

$$C_{BOOT} \geq 10 \times C_g \geq 76\text{nF} \tag{5}$$

For this design example a 100-nF capacitor was chosen for the bootstrap capacitor.

$$C_{BOOT} = 100\text{ nF} \tag{6}$$

9.2.2.3 Selecting VDD Bypass/Holdup Capacitor (C_{VDD}) and R_{bias}

The VDD capacitor (C_{VDD}) should be chosen to be at least 10 times larger than C_{BOOT}. For this design example a 1-µF capacitor was selected.

$$CVDD \geq 10 \times C_{BOOT} = 1\,\mu F \tag{7}$$

A 5-Ω resistor R_{BIAS} in series with bias supply and VDD pin is recommended to make the VDD ramp up time larger than 50 µs to prevent error logic error spikes on the outputs as shown in Figure 55

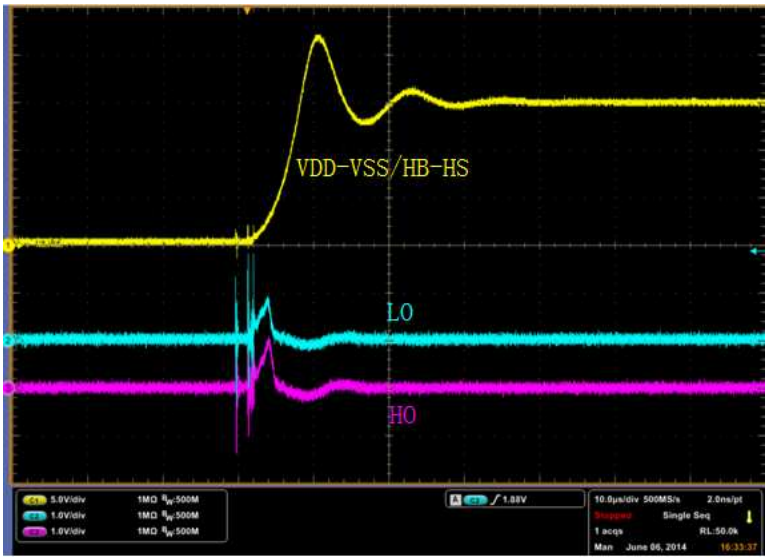


Figure 55. VDD/HB-HS Fast Ramp Up

9.2.2.4 Selecting Bootstrap Resistor (R_{BOOT})

Resistor R_{BOOT} is selected to limit the current in D_{BOOT} and limit the ramp up slew rate of voltage of HB-HS to avoid the phenomenon shown in Figure 55. It is recommended when using the UCC27714 that R_{BOOT} is between 2 Ω and 10 Ω. For this design we selected a current limiting resistor of 2.2 Ω. The bootstrap diode current ($I_{DBOOT(pk)}$) was limited to roughly 5.2 A.

$$R_{BOOT} = 2.2\ \Omega \tag{8}$$

$$I_{DBOOT(pk)} = \frac{VDD - V_{DBOOT}}{R_{BOOT}} = \frac{12\ V - 0.6\ V}{2.2\ \Omega} \approx 5.2\ A \tag{9}$$

The power dissipation capability of the bootstrap resistor is important. The bootstrap resistor must be able to withstand the short period of high power dissipation during the initial charging sequence of the boot-strap capacitor. This energy is equivalent to 1/2 × CBOOT × V^2. This energy is dissipated during the charging time of the bootstrap capacitor (~3 × R_{BOOT} × C_{BOOT}). Special attention must be paid to use a bigger size R_{BOOT} when a bigger value of C_{BOOT} is chosen.

9.2.2.5 Selecting Gate Resistor R_{HO}/R_{LO}

Resistor R_{HO} and R_{LO} are sized to reduce ringing caused by parasitic inductances and capacitances and also to limit the current coming out of the gate driver. For this design 3.01-Ω resistors were selected for this design.

$$R_{HO} = R_{LO} = 3.01\,\Omega \tag{10}$$

Maximum HO Drive Current (I_{HO_DR}):

$$I_{HO(dr)} = \frac{V_{VDD} - V_{DBOOT}}{R_{HO} + R_{HOH}} = \frac{12\ V = 0.6\ V}{3.01\,\Omega + 3.75\ \Omega} \approx 1.7\ A \tag{11}$$

Maximum HO Sink Current (I_{HO_SK}):

$$I_{HO(sk)} = \frac{V_{VDD} - V_{DBOOT}}{R_{HO} + R_{HOL}} = \frac{12\ V = 0.6\ V}{3.01\,\Omega + 1.45\ \Omega} \approx 2.6\ A \tag{12}$$

Maximum LO Drive Current (I_{LO_DR}):

$$I_{LO(dr)} = \frac{V_{VDD}}{R_{LO} + R_{LOH}} = \frac{12\ V}{3.01\,\Omega + 3.75\ \Omega} \approx 1.8\ A \tag{13}$$

Maximum LO Sink Current (I_{LO_SK}):

$$I_{LO(sk)} = \frac{V_{VDD}}{R_{LO} + R_{LOL}} = \frac{12\ V}{3.01\,\Omega + 1.45\ \Omega} \approx 2.7\ A \tag{14}$$

9.2.2.6 Selecting Bootstrap Diode

A fast recovery diode should be chosen to avoid charge is taken away from the bootstrap capacitor. Thus, a fast reverse recovery time t_{RR}, low forward voltage V_F and low junction capacitance is recommended.

Suggested parts include MURA160T3G and BYG20J.

9.2.2.7 Estimate the UCC27714 Power Losses ($P_{UCC27714}$)

The power losses of UCC27714 ($P_{UCC27714}$) are estimated by calculating losses from several components:

The static power losses due to quiescent current (I_{QDD}, I_{QBS}) are calculated in Equation 15:

$$P_{QC} = V_{VDD} \times (I_{QDD} + I_{QBS}) \quad (15)$$

Static losses due to leakage current (I_{BL}) are calculated from the HB high-voltage node as shown in Equation 16:

$$P_{I_{BL}} = V_{HB} \times I_{BL} \times D \quad (16)$$

Dynamic losses incurred due to the gate charge while driving the FETs Q1 and Q2 are calculated Equation 17. Please note that this component typically dominates over the dynamic losses related to the internal VDD & VHB switching logic circuitry in UCC27714.

$$P_{Q_{G1},Q_{G2}} = 2 \times V_{VDD} \times Q_G \times f_{SW} \quad (17)$$

Equation 18 calculates dynamic losses during the operation of the level shifter at HO turn-off edge. Q_P, typically 0.5 nC, is the charge absorbed by the level shifter during operation at each edge. Please note that if high-voltage switching occurs during HO turn-on as well (as in the case of ZVS topologies), then the power loss due to this component must be effectively doubled.

$$P_{LevelShift} = V_{HB} \times Q_P \times f_{SW} \quad (18)$$

The total power losses are calculated in Equation 19:

$$P_{UCC27714} \approx V_{VDD} \times (I_{QDD} + I_{QBS}) + V_{HB} \times I_{BL} \times D + 2 \times V_{VDD} \times Q_Q \times f_{SW} + V_{HB} \times Q_P \times f_{SW} \quad (19)$$

For the conditions, VDD=VBS=15V, VHB = VHS + VBS = 400V, HO On-state Duty cycle D = 50%, Q_G = 87nC, f_{SW} = 100kHz, the total power loss in UCC27714 driver for a ZVS power supply topology can be estimated as follows, assuming no external gate drive resistors are used in the design:

$$P_{UCC27714} \approx 15\ V \times (750\ \mu A + 120\ \mu A) + 400\ V \times 20\ \mu A \times 0.5 + 2 \times 15\ V \times 87\ nC \times 100\ kHz + 2 \times 400\ V \times 0.5\ nC \times 100\ kHz = 0.318\ W \quad (20)$$

When external resistors are used in the gate drive circuit, a portion of this power loss is incurred on these external resistors and the power loss in UCC27714 will be lower, allowing the device to run at lower temperatures.

9.2.2.8 Application Example Schematic Note

In the application example schematic there are 10-kΩ resistors across the gate and source terminals of FET Q1 and Q2. These resistors are placed across these nodes to ensure FETs Q1 and Q2 are not turned on if the UCC27714 is not in place or properly soldered to the circuit board or if UCC27714 is in an unbiased state.

9.2.3 Application Curves

Figure 56 and Figure 57 show the measured LI to LO turn-on and turn-off delay of one UCC27714 device. Channel 1 depicts VDD, Channel 2 LO and Channel 3 LI.

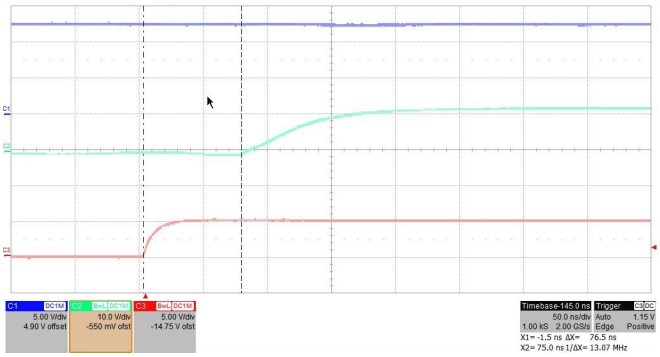


Figure 56. LI to LO Turn-On Propagation Delay

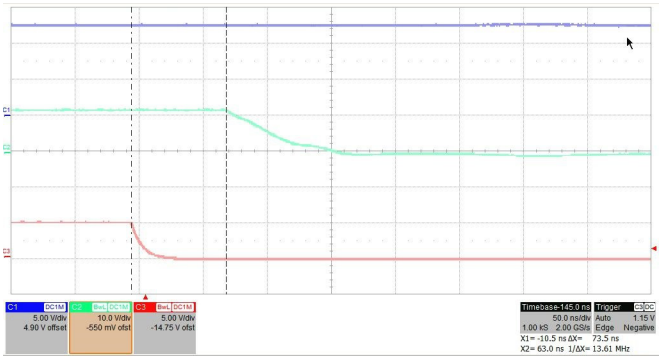


Figure 57. LI to LO Turn-Off Propagation Delay

Figure 58 and Figure 59 show the measured HI to HO turn-on and turn-off delay of one UCC27714 device. Channel 1 depicts HI, Channel 2 LO, Channel 3 HO and Channel 4 VDD.

NOTE

HO was measured with a 1:20 differential probe.

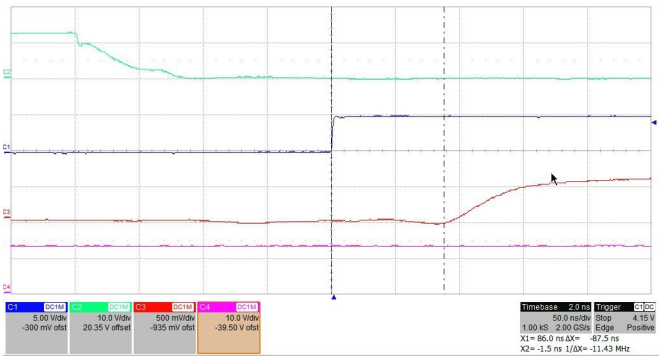


Figure 58. HI to HO Turn-On Propagation Delay

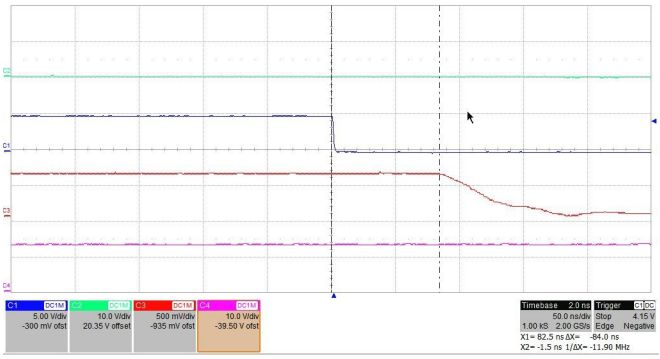


Figure 59. HI to HO Turn-Off Propagation Delay

10 Power Supply Recommendations

The VDD power terminal for the device requires the placement of electrolytic capacitor as energy storage capacitor, because of UCC27714 is 4-A, peak-current driver. And requires the placement of low-esr noise-decoupling capacitance as directly as possible from the VDD terminal to the VSS terminal, ceramic capacitors with stable dielectric characteristics over temperature are recommended, such as X7R or better.

The recommended e-capacitor is a 22-µF, 50-V capacitor. The recommended decoupling capacitors are a 1-µF 0805-sized 50-V X7R capacitor, ideally with (but not essential) a second smaller parallel 100-nF 0603-sized 50-V X7R capacitor.

Similarly, a low-esr X7R capacitance is recommended for the HB-HS power terminals which must be placed as close as possible to device pins.

As described earlier in VDD and Under Voltage Lockout, the attention must be exercised to ensure that the VDD-VSS bias voltage does not dip from $VDD_{(OFF)}$ to 4-V level in 70 µs or less

11 Layout

11.1 Layout Guidelines

- Locate UCC27714 as close as possible to the MOSFETs in order to minimize the length of high-current traces between the HO/LO and the Gate of MOSFETs.
- A 5-Ω resistor series with bias supply and VDD pin is recommended.
- Locate the VDD capacitor (C_VDD) and VHB capacitor (CBS) as close as possible to the pins of UCC27714.
- A 2-Ω to 5-Ω resistor series with bootstrap diode is recommended to limit bootstrap current.
- A RC filter with 5.1 Ω to 51 Ω and 220 pF for HI/LI is recommended.
- Separate power traces and signal traces, such as output and input signals.

11.2 Layout Example

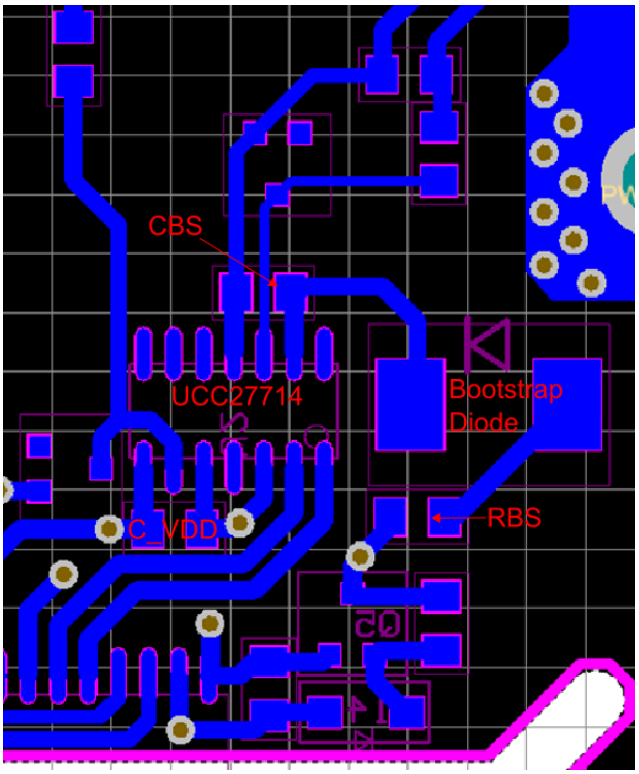


Figure 60. UCC27714 Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

User Guide, *Using the UCC27714EVM-551*, (SLUUB02)

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27714D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC27714	Samples
UCC27714DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC27714	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

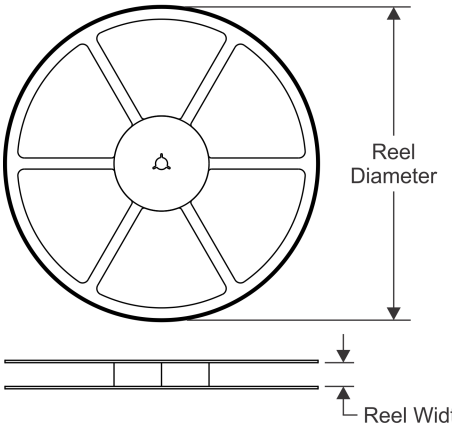
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

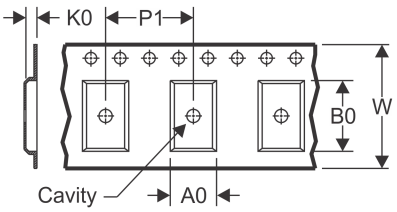
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

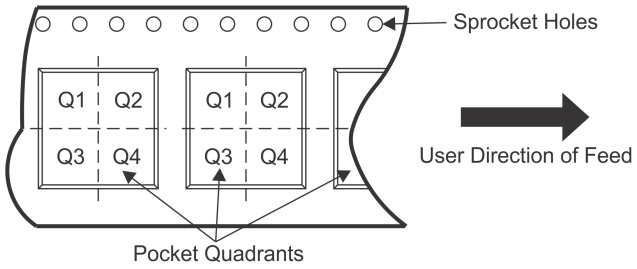


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

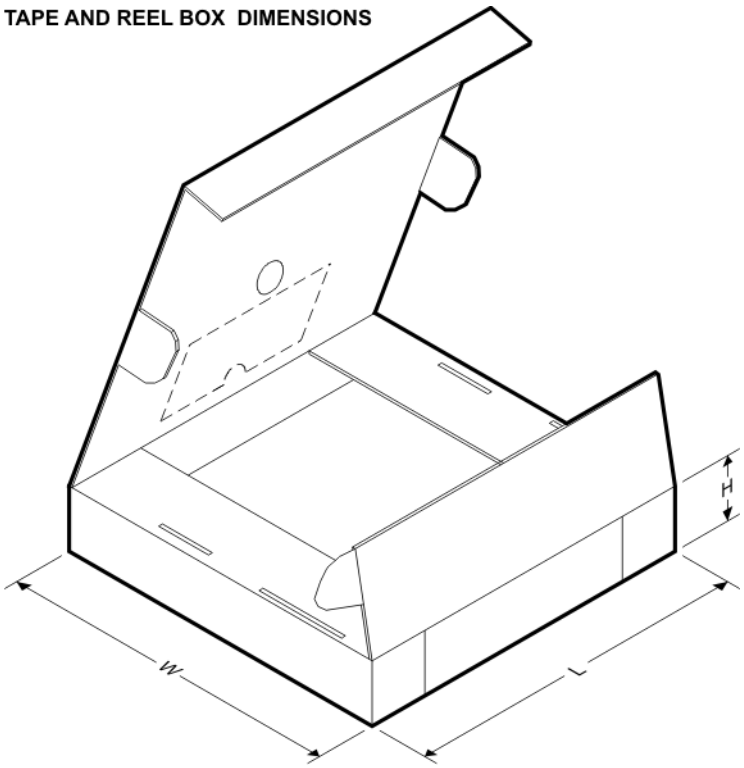
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27714DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

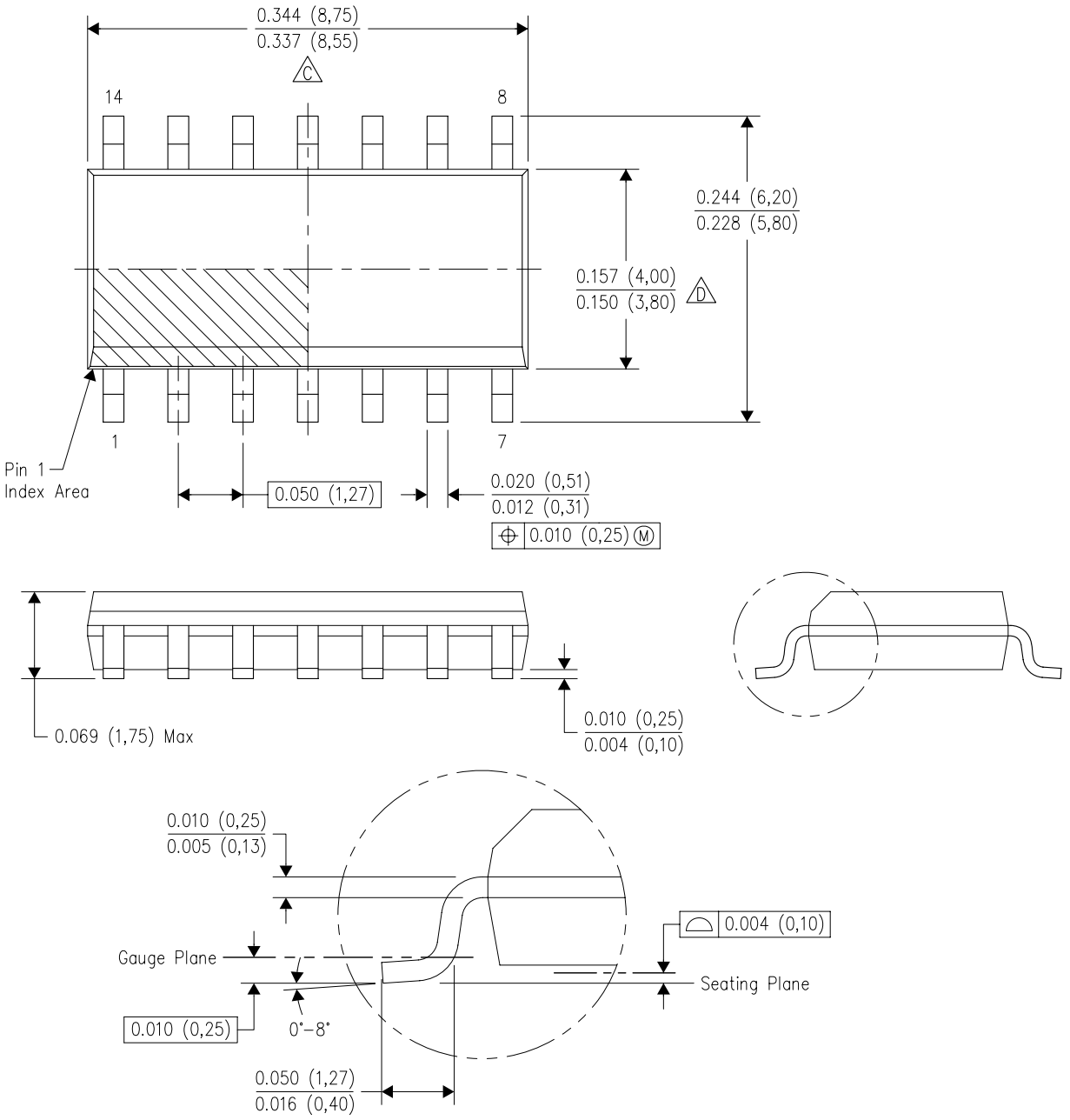
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27714DR	SOIC	D	14	2500	367.0	367.0	38.0

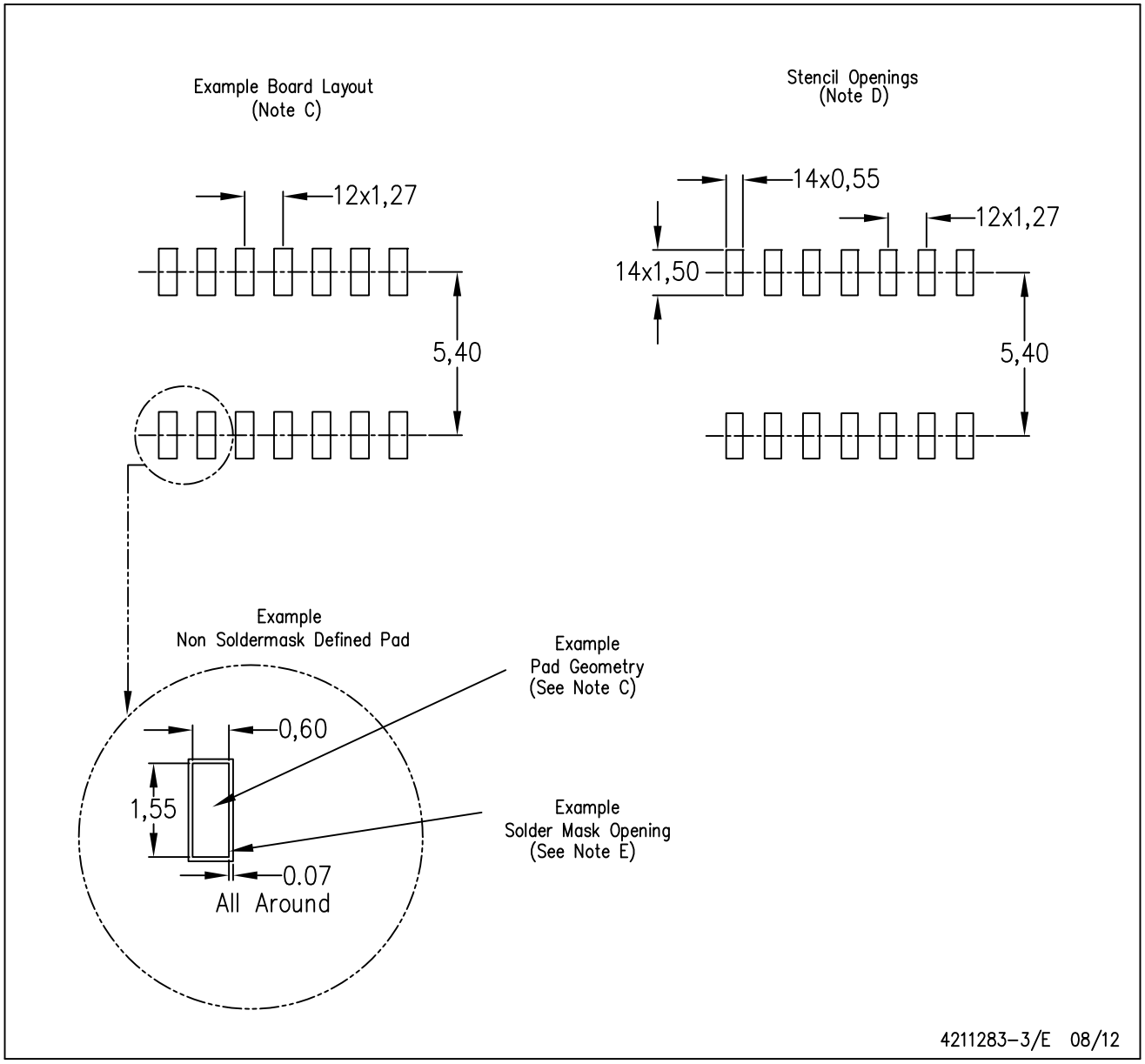
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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